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Development of overcurrent relay model and power system simulator using National Instruments devices in real-time

Sunil Kumar Palla

DEVELOPMENT OF OVERCURRENT RELAY MODEL AND POWER SYSTEM SIMULATOR USING NATIONAL INSTRUMENTS DEVICES IN REAL-TIME

By

Sunil Kumar Palla

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By

Sunil Kumar Palla

Approved:

Anurag K. Srivastava
Assistant Research Professor of Electrical and Computer Engineering
(Director of Thesis)

Noel N. Schulz
Professor of Electrical and Computer Engineering
(Committee Member)

Herbert L. Ginn
Assistant Professor of Electrical and Computer Engineering
(Committee Member)

James E. Fowler
Professor and Interim Director of Graduate Studies, Electrical and Computer Engineering

Sarah A. Rajala
Dean of Bagley College of Engineering

Name: Sunil Kumar Palla

Date of Degree: December 12, 2008

Institution: Mississippi State University

Major Field: Electrical Engineering

Major Professor: Dr Anurag K. Srivastava

Title of Study: DEVELOPMENT OF OVERCURRENT RELAY MODEL AND POWER SYSTEM SIMULATOR USING NATIONAL INSTRUMENTS DEVICES IN REAL-TIME

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Candidate for Master of Science

One of the major objectives at Mississippi State University's Power and Energy Research Laboratory (PERL) is to develop an adaptive protective controller for Shipboard Power System (SPS) protection. This thesis work focuses on developing an overcurrent relay model in LabVIEW and validating the model by conducting HIL tests with RTDS and SEL-351S over-current relay.

This thesis also proposes a high-performance and low-cost National Instruments-PXI platform for power system simulations. Two-bus, eight-bus and shipboard power system (SPS) test cases are developed using Matlab/Simulink. To determine the performance of NI-PXI system, open loop tests are done between NI-PXI acting as power system simulator and SEL-351S relay and these results are compared with the results of similar test conducted between RTDS and SEL-351S relay. HIL tests are done between NI-PXI system and dSPACE relay model, NI-PXI and SEL-351S relay. These results show that NI-PXI controller can be used as a power system simulator.

DEDICATION

I would like to dedicate this research work to my parents and my advisor.

ACKNOWLEDGMENTS

I would like to add a few heartfelt words for the people who were part of this research in numerous ways. I wish to express my deep sense of gratitude to my major professor, Dr. Anurag K. Srivastava, for his keen interest and assistance offered towards this research. I would like to convey my sincere thanks to other committee members, Dr. Noel N Schulz and Dr. Herbert Ginn for their valuable support.

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INTRODUCTION

1.1 Shipboard Power Systems

The Shipboard Power System (SPS) is very important on an electric ship for supplying power to carry out most of its major operations [1]. Future naval ships require significantly larger amounts of energy due to loads, such as pulsed weapons and Electromagnetic Aircraft Launch System (EMALS) [2]. There is a need for efficient and economical design of SPS to meet the requirements for high-energy demand.

Modeling and simulation of devices used on SPS for different conditions are needed for better design. Real-time platforms can address the needs partially by testing the developed device models in real-time. The tested models can be further integrated to perform an overall simulation for different operating conditions. This work focuses on development of a protective relay model and developing a real-time Hardware-in-the-loop (HIL) simulation platform.

1.2 Protective Relaying

Continuity of service is a vital operational goal in SPS. Upon occurrence of a fault, the protection devices should disconnect the faulted part to keep the rest of the

system operating. Satisfactory performance of protection system components, such as a protective relay, is of great importance. The aim of protective relays is to detect abnormal conditions or defective equipment and initiate actions to disconnect faulted parts of the system and thus protect the power system from detrimental power system conditions, such as high currents, over/under voltages, and over/under frequency [3].

1.3 Hardware-in-the-Loop Simulation

Shipboard Power Systems (SPS) consist of various vital devices and these devices have to be tested under different conditions. The real-time Hardware in the Loop (HIL) test provides a platform to test the performance of the equipment under different conditions and obtain its response [2][4]. Recently, more emphasis has been given to real-time HIL simulation as the devices can be tested under virtual real operating conditions. This type of testing is very important for devices on SPS, because the performance of SPS is dependent on the operational reliability of each device used.

1.4 Previous Work

This section of the chapter provides a survey of previous work done on protective relay modeling and on real-time HIL platform development.

1.4.1 Modeling of protective relay

Reference [5] proposes a transient power system program, which can embed a relay simulation (algorithm). The transient power system program allows the testing of

relay models for different fault scenarios. A directional overcurrent relay model is considered and it is embedded into the power system program. The overcurrent relay model is tested for phase-A to ground fault at different locations on the power system [5].

Authors in [6] presented a modeling package for generating relay models. The relay-modeling package consists of two modules. The specifications collection module is used to collect the detailed specifications needed for the relay design from the user. Using this data, the generation module generates the required relay model. The resultant relay model code will be generated using Matlab software. The relay-modeling package is validated for an overcurrent relay and distance relay. Test signals are generated using a real-time playback simulator (RTPS). These test signals are fed to physical relays and their response is observed. Similar signals are fed to generated over-current and distance relay models and their response is also observed. As a validation process, the results of physical relays and generated relay models were compared [6].

Mladen Kezunovic et al. [7] developed user-friendly software for protective relaying applications and design concepts. The Matlab software with Simulink support and power block set (PBS) toolbox of Matlab is used to develop customized user libraries, which contains all the relay elements as subsystems [7]. Using these libraries, the user can build any relay model and test it.

Reference [8] proposes an impedance relay model. The impedance relay model is developed in RSCAD. The model is subjected to testing with a power system model developed in RSCAD itself [8].

Daxa Patel et al. [9] developed an instantaneous overcurrent relay model in the Virtual Test Bed (VTB). To verify the performance of the VTB model, a radial power system was built in VTB. The relay model was tested for different faults placed on the power system. The developed overcurrent relay model was validated by design of a similar relay model in Matlab/Simulink and was tested for various fault conditions [9].

In the literature, the majority of the articles on relay modeling used the Matlab/Simulink environment for designing the respective algorithm or model. The developed models are subjected to testing for various fault scenarios in the Matlab environment. None of the articles, except reference [8] were implemented in real-time for better testing and analysis by simulating the real operating conditions.

1.4.2 Real-time Power HIL platform

B.S.Rigby et al. [10] demonstrate the use of Real-Time Digital Simulator (RTDS) [11] for conducting a closed loop test with a SEL-311C relay acting as an overcurrent relay. A radial power system is built in RSCAD with faults inserted at different parts of the system. A closed loop test is conducted by running the power system on RTDS with SEL-311C connected to the RTDS terminals. Performance of the relay is observed for faults on different parts of the system. This article gives major emphasis on modeling issues and hardware requirements for conducting closed loop relay testing.

Reference [12] demonstrates HIL testing between RTDS and SEL-421 impedance relay. An eight-bus power system is used in this testing. The test case is run in real-time with the relay connected to the RTDS. HIL test is conducted for L-G and L-L-G faults.

Daxa Patel [9] worked with the VTB-RT platform. An RLC circuit was designed in VTB and later implemented in VTB-RT to conduct a real-time HIL test with a PI controller running on dSPACE [9]. Reference [13] proposes a fast, low-cost testing procedure for digital controller design using real-time HIL simulation. The real-time HIL simulation is conducted making use of VTB-RT platform.

1.4.3 Application of National Instruments products in Power Systems

Reference [14] presents a real-time test bed developed to study the real time issues that arise during the design of new control and stability methodologies for shipboard power systems. The power system model is run on desktop ETS (Embedded Tool suite) in real-time and respective voltages and currents are sent to the reconfigurable and control methods, which are run in real-time on compact Reconfigurable I/O (cRIO) and Field Programmable Gate Array (FPGA) devices. The switch states and switch control signals given by the reconfigurable methods are fed back to the power system that performs the required reconfiguration [14].

Reference [15] uses National Instrument PXI, NI DAQ cards for conducting an HIL to test the shunt active compensator performance in real-time. Reference [16] presents the use of National Instruments software for the design of static VAR Compensator controller for unbalanced industrial loads. The software code for the controller is developed in LabVIEW real-time. NI cards are used to sample the three phase voltages and currents and give triggering pulses [16].

1.5 Thesis Objective

This thesis makes contributions towards protective relay modeling and real-time hardware in the loop simulation.

At Mississippi State University efforts are in progress to develop an adaptive protective controller for Shipboard Power System (SPS) protection that can adapt different protective schemes as needed. The first step of this process is overcurrent and differential relay model development using different platforms [12]. This thesis outlines efforts to meet these needs for real time simulation by addressing an overcurrent relay model in LabVIEW [13] and running it in real-time on NI-PXI system. LabVIEW graphical programming language is used here considering its design ease and flexibility. It has various built-in functions and debugging techniques that will be useful to optimize the speed and performance of the LabVIEW application [17]. Moreover, NI-PXI is a high-performance and low-cost PC-based platform used for measurement and automation systems including power and control applications [18] [19] [20]. These systems serve applications such as manufacturing tests, military and aerospace, machine monitoring, automotive, and industrial tests. The upper branch of the Figure 1.1 shows NI-PXI platform being used as overcurrent relay simulator.

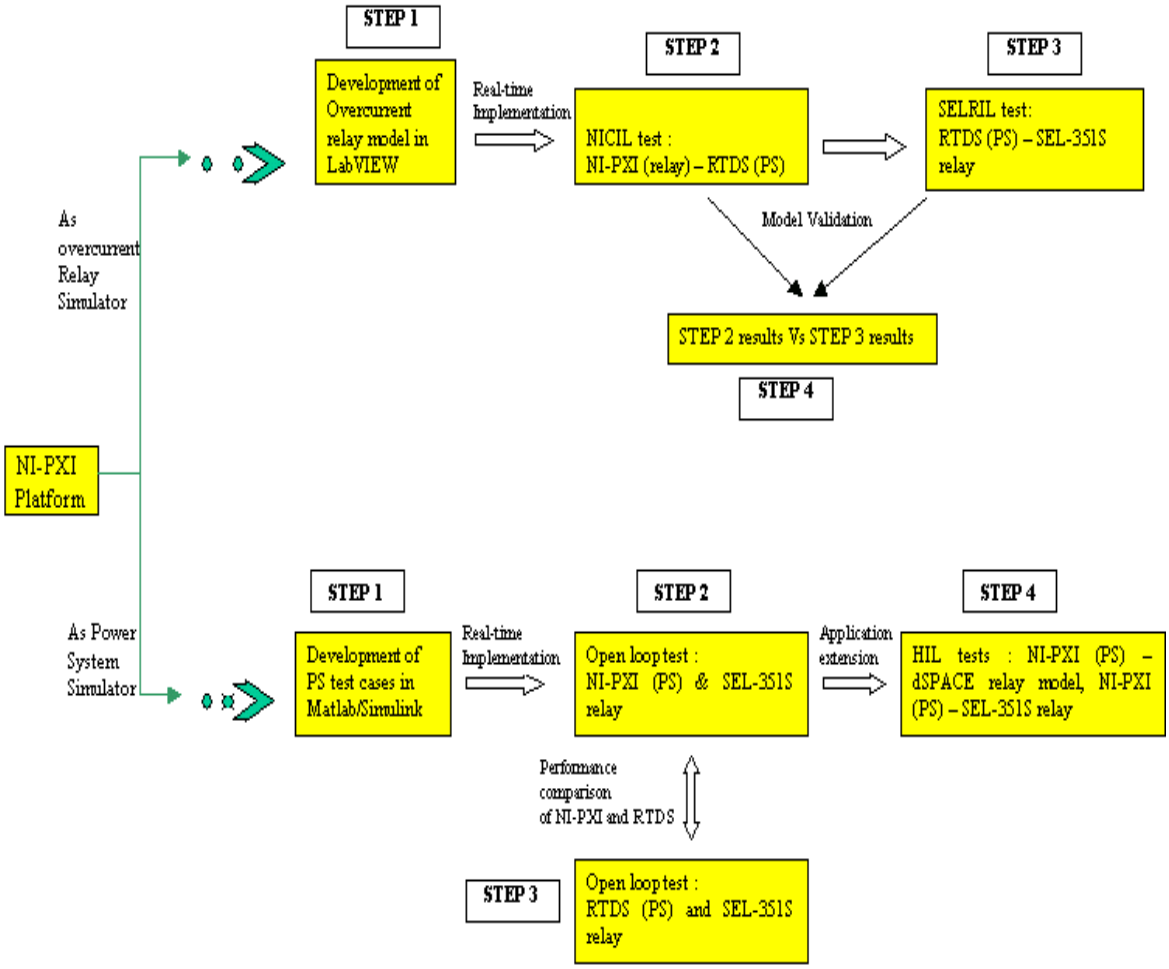


Figure 1.1 Overview of this thesis work

This research work also attempts to develop a robust, rapid and low cost HIL simulation platform using NI-PXI system. The lower branch of the Figure 1.1 shows NI-PXI platform being used as power system simulator (PSS). Efforts have been placed to establish NI-PXI as a power system simulator by conducting open loop tests and later validating those results with the open loop test conducted with the RTDS [21]. HIL tests are also conducted between NI-PXI PSS and a SEL relay as well as a dSPACE relay model [22].

1.6 Thesis Organization

This thesis is organized into eight chapters. Chapter I provides introduction to the work and presents the literature review. Chapter II provides the necessary background for this work. Chapter III presents the Matlab/Simulink test cases for two-bus, eight-bus and shipboard system. The eight-bus system test case in RSCAD is also presented. Chapter IV details the development of overcurrent relay model in LabVIEW.

Chapter V presents the results for Software-in-the-Loop test conducted between the Matlab/Simulink power system test cases and Matlab/Simulink relay model. Chapter VI deals with results of closed loop tests conducted between RTDS and LabVIEW relay model. For validation purpose, a HIL test is conducted between RTDS and SEL-351S and its results are compared with closed loop test results for similar faults. Chapter VII establishes NI-PXI as a power system simulator. Performance analysis of an NI-PXI controller is done by conducting open loop tests between NI-PXI and SEL-351S overcurrent relay and between RTDS and SEL-351S. A HIL test is conducted between NI-PXI and dSPACE with the power system model running on NI-PXI and overcurrent relay model running on dSPACE. This test is done for different power system models for several fault conditions. The results of HIL testing between NI-PXI acting as power system and SEL-351S relay are also presented. Finally, Chapter VIII concludes the thesis and suggests some future work.

CHAPTER II

BACKGROUND

2.1 Introduction

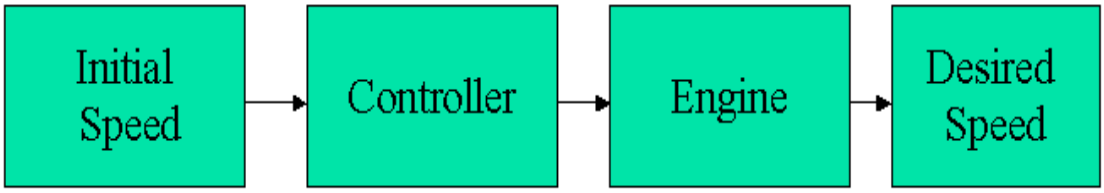
This chapter gives an insight into various topics related to this research work. Details about modeling, computer simulation, real-time simulation, Hardware-in-the-Loop (HIL) simulation and data acquisition are presented here. An overview of software tools, RSCAD, LabVIEW and Simulink, are given. LabVIEW, LabVIEW Real-Time (LabVIEW RT) and a major add-on for LabVIEW, NI Simulation interface toolkit (SIT) are extensively used for modeling and real-time simulation purposes in this work. Measurement and Automation Explorer software used along with NI hardware is discussed. In-depth discussions about different real-time simulators including RTDS, NI-PXI AND dSPACE used for this thesis work are presented.

2.2 Terms and Definition

2.2.1 Modeling

System modeling can be defined as study of mechanisms inside a system [23]. Modeling is a representation of reality. If a model is implemented in computer software,

it is known as a computerized model. Modeling is needed for understanding, analysis, and design. Models should be inferred using basic laws and relationships and should never be confused with a real physical system [23]. Figure 2.1 shows the mathematical model for the cruise control of a car.



Mathematical model

$$m\dot{v} = F_{acc} + \ldots$$
$$J_f\ddot{\theta} = M_f i_f - b_f\dot{\theta} + \ldots$$
$$Ci_b = i_b + \ldots$$

Figure 2.1 Mathematical model for the cruise control of a car [23]

2.2.2 Simulation

Simulation is the imitation of a real system [24]. These simulations show how a system behaves for different operating conditions. There are varieties of computer software used for simulations depending on the application. If a simulation involves real-time data for prediction of system behavior then it is classified as real-time simulation. Real-time simulators deal with real-time simulations. Some of the real-time simulators include RTDS, NI-PXI, and dSPACE etc. Real-time simulations are extremely useful and

preferred when compared to ordinary computer simulations because it generally involves dealing with real-time signals.

2.2.3 Hardware-in-the-Loop (HIL) Test

HIL simulation refers to a system in which parts of a pure simulation have been replaced with the actual physical components. A HIL test helps in understanding the behavior of new devices under different operating conditions. It also helps in building an ideal model and validates the model for a new device [2], [25], [26]. Figure 2.2 clearly explains the concept of HIL testing.

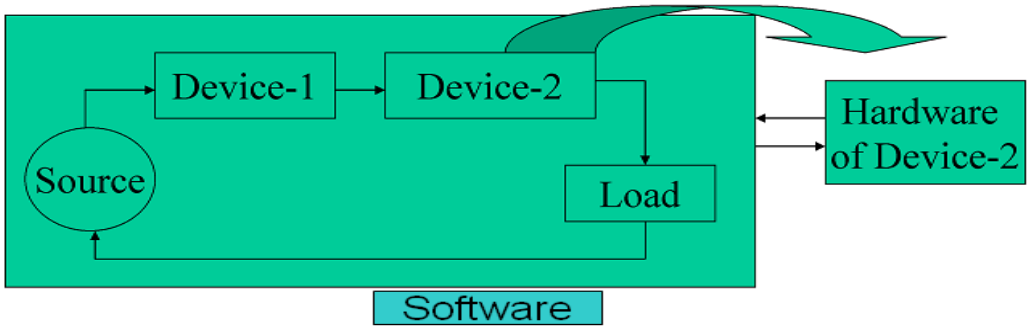


Figure 2.2 HIL test.

Consider a system with a source, device-1, device-2 and a load. Assume that the entire system is built using simulation software. To know, how device-2 behaves in the real world, replace device-2 with its real hardware. Have the remaining system to run in real-time using a real-time simulator such as RTDS and connect the real hardware of device-2 to the real-time simulator. This kind of simulation is known as Hardware-in-the-

Loop (HIL) simulation and helps in predicting the behavior of device-2 for a given system state.

Real-time HIL simulation is becoming an essential simulation tool for engineering design, especially in protection equipment, automotive, controls, and power electronics design [4]. A terrestrial or Shipboard Power System (SPS) consists of various vital devices such as generators, relays, transformers, and pulse loads. Each device will have different characteristics and these devices have to be tested under different conditions. The HIL test provides a platform to test the performance of the equipment under different conditions and obtain its response.

2.2.4 Data Acquisition

Data acquisition (DAQ) is defined as the process of gathering real-world signals and converting them into digital form for storage, analysis or presentation on a computer [27]. These real world signals can be voltage, temperature, pressure etc. Figure 2.3 shows a data acquisition system.

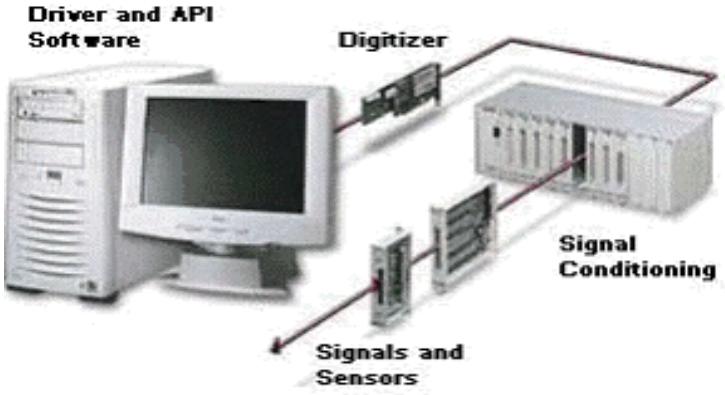


Figure 2.3 Data Acquisition System [27]

The process of data acquisition begins with transducers. Appropriate transducers (sensors) convert the real world signals into representative electrical signals. These electrical signals can be high voltages and noisy. For this purpose, signal conditioning is a must. This assures safety and accuracy of the signal being acquired. The conditioned signal is converted into digital form for the purpose of storage, manipulation or presentation on the computer [27].

2.3 Software Tools

2.3.1 RSCAD

RSCAD is powerful Graphical User Interface (GUI) software that allows the users to build test cases by using the different components present in the RSCAD library [11]. The main application of this software is for power systems. The designed models can be run on RTDS in real-time. The RSCAD power system component library consists of sources, transmission lines, HVDC, machines, transformers (both instrument and power), series compensation, and Flexible Alternating Current Transmission Systems (FACTS). Through RSCAD, the user is able to construct, run, and analyze the simulation cases [11]. The file manager window in the RSCAD has 'Draft', 'Runtime', 'Multiplot', 'Cable', 'T-Line, 'Help', 'Convert' and 'Manuals' menus. The power system can be built using the Draft and the model libraries present in the draft file [12].

2.3.2 National Instruments LabVIEW

LabVIEW (Laboratory Virtual Instrument Engineering Workbench), developed by National Instruments (NI), is a graphical programming language that is user friendly and is used to develop complex measurement and control applications very quickly and easily. LabVIEW programs are called virtual instruments (VIs) because their appearance and operation imitate actual instruments. A LabVIEW VI contains three main parts.

- Front Panel.
- Block Diagram.
- Icon/Connector.

The front panel is the interactive user interface of a VI. The front panel consists of controls and indicators, whose values will be updated from the block diagram of that VI. The block diagram is the actual executable program. The controls and indicators that were placed on the front panel appear as terminals on the block diagram. Apart from these, the block diagram can contain functions (built-in and user defined) and structures to perform the necessary task [28]. A VI can be used as a subroutine in another VI block diagram. If a VI has to be used as a subroutine then it must have an icon and a connector. A VI that is used within another VI is called a sub VI. A VI's connector is the mechanism used to wire data into the VI from other block diagrams when the VI is used as a sub VI [18].

2.3.3 Measurement and Automation Explorer

Measurement & Automation Explorer is abbreviated to MAX. Figure 2.4 shows the MAX window. It helps to view the National Instrument (NI) devices and systems

connected and installed software in those devices and systems. It enables the user to modify/delete the software. MAX also helps in calibrating the NI devices. The user can create, edit and scale virtual instruments using MAX [29]. Figure 2.5 shows the software present on host computer as well as remote real-time target.

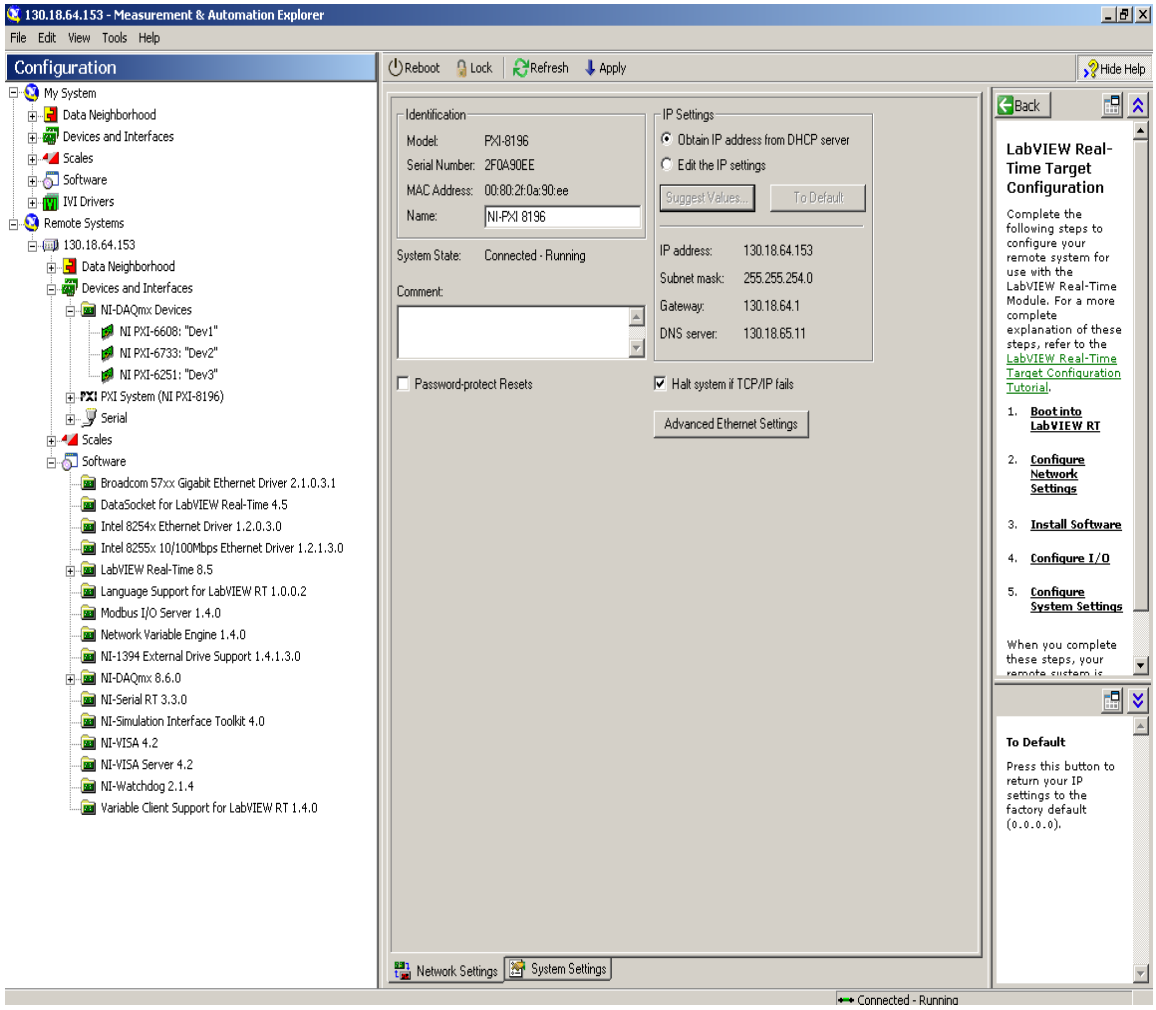


Figure 2.4 MAX software window

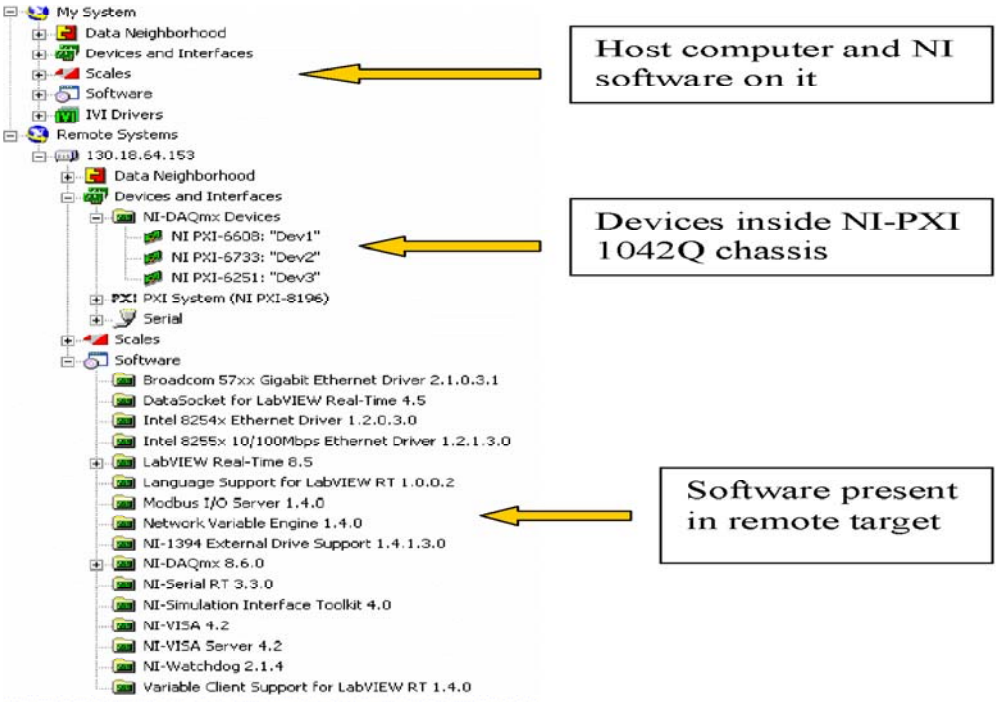


Figure 2.5 MAX window showing NI software and hardware.

2.3.4 National Instruments LabVIEW SIT

The LabVIEW Simulation Interface Toolkit (SIT) permits the use of LabVIEW with Matlab/Simulink and real time workshop. Combination of LabVIEW along with Matlab/Simulink allows the users to develop, prototype and test different systems using models developed in Matlab/Simulink [30]. At the Mississippi State University Power and Energy Research Laboratory (MSU PERL), computers are equipped with SIT 4.0 version.

To install the SIT 4.0, the following software versions must be installed on the computer [31]:

- National Instruments LabVIEW 8.5 Full or Professional Development System

- The Math Works, Inc. MATLAB® / Simulink® application software release 13.*x*, 14.*x*, or 2006a, 2006b, 2007a
- The Math Works, Inc. Real-Time Workshop® release 13.*x*, 14.*x* or 2006a, 2006b, 2007a
- Microsoft Visual C++ 6.0 or .NET 2003.

To run the models on various real-time targets, real-time workshop, an add-on package for Simulink is used. The real-time workshop generates the C code from Simulink models and then uses a C compiler to compile the C code for execution on the real-time target.

2.3.5 National Instruments Real-Time

NI LabVIEW real-time module combines the LabVIEW graphical environment with LabVIEW real-time targets such as NI-PXI, and FPGA. With this real-time module, the user can monitor and simulate a physical system, repeatedly performing a particular task with a specified time interval in a deterministic manner [18] [19]. The LabVIEW real-time will ensure that it has direct control of all the tasks on the real-time target. The execution of higher priority tasks first will be guaranteed with absolute reliability on the real-time targets [18] [19]. Figure 2.5 shows that at the MSU PERL, the deployment platform is NI-PXI and LabVIEW Real-Time 8.5 is installed on it.

2.3.6 Host Computer and Remote Real-Time Target

The host computer is a computer with an operating system (OS), such as Microsoft Windows, Linux and LabVIEW professional software installed on it. The user

creates the LabVIEW user interface on the host computer [30]. Remote real-time target can be a NI-PXI, Compact RIO or another host with real-time OS. LabVIEW VI can be deployed into a remote real-time target for running the VI in real-time.

2.4 Real-Time Controllers/Simulators

2.4.1 National Instruments-PXI Controller

The NI-PXI system is a rugged, high-performance and low-cost PC-based platform for measurement and automation systems. These systems serve applications such as manufacturing tests, military and aerospace, machine monitoring, automotive, and industrial tests. The hardware architecture of NI PXI system consists of three basic components – chassis, system controller, and peripheral modules [18].

MSU PERL is equipped with NI-PXI system, shown in Figure 2.6. LabVIEW graphical programming language is used to interact with NI-PXI. Devices such as NI-PXI 8196 controller, NI-PXI 6251, NI-PXI 6608, and NI-PXI 5412 occupy this NI-PXI system chassis slots.

Figure 2.6 NI-PXI system with an 8 slot chassis

This NI- PXI chassis contains NI PXI 8196 system controller at slot-1. Figure 2.7 shows a NI-PXI 8196 controller. The controller at MSU PERL consists of Intel (R) Pentium (R) M processor with a CPU speed of 2GHz and a RAM of 1GB. It also has four USB 2.0 ports, an Express Card slot, an integrated hard drive, GPIB, serial and parallel communication ports. Development and operation of Windows-based PXI systems is not much different from that of a standard Windows-based PC [26] [18].

Figure 2.7 NI-PXI 8196 Controller [26] [18]

The NI-PXI 6608 is a High-Precision Counter/Timer with Digital I/O. Figure 2.8 shows a NI-PXI 6608 device. It is an eight-channel, 32-bit up/down counter/ timer module. Eight digital I/O lines are dedicated and the remaining 24 are shared with the counter/timers. A wide variety of counter/timer tasks such as event counting, period measurement, pulse-width measurement, pulse generation, pulse-train generation, and frequency measurement can be done [26] [18].

Figure 2.8 NI-PXI 6608 [26] [18]

The NI-PXI 6251 is an M series multifunctional DAQ card. Figure 2.9 shows an NI-PXI 6251 device. It has sixteen analog inputs with a maximum data acquisition rate of 1.25 M Samples/s, two analog outputs, and twenty-four digital I/O lines. It also has channels for analog and digital triggering [26] [18].

Figure 2.9 NI-PXI 6251 [26] [18]

The NI-PXI-5412 is a waveform generator. Figure 2.10 shows a NI-PXI 5412 device. It has a sampling rate of 100 M samples/s. It can download waveforms faster than GPIB instruments. It can do waveform analysis [26] [18].

Figure 2.10 NI-PXI 5412 [26] [18].

2.4.2 Real Time Digital Simulator (RTDS)

RTDS is a real-time power system simulator, which employs an advanced, and easy to use graphical user interface. The RTDS allows users to accurately develop their models and simulate them efficiently.

Figure 2.11 Real Time Digital Simulator

RTDS is capable of generating the real time signals, which enables the user to simulate the real time power system scenarios. Figure 2.11 shows the RTDS at MSU PERL. The RTDS has its applications spread over a wide range of area.

RTDS hardware is based on Digital Signal Processor (DSP) and Reduced Instruction Set Computer (RISC), which utilize advanced parallel processing techniques in order to achieve computational speeds required to maintain continuous real-time operation. Each rack of RTDS can have three types of processor cards namely, 3PC, GPC, and RPC. The Triple Processor Card (3PC) consists of 3 independent Analog Digital Signal Processor (ADSP21062). The RISC Processor card (RPC) consists of two IBM PowerPC 750CXe processors. The Giga Processor Card (GPC) contains two IBM PowerPC 750GX processors. The RTDS simulator may consist of 3PC only or a combination of 3PC, GPC and RPC [11].

2.4.3 dSPACE

dSPACE is a real-time platform consisting of a PowerPC processor, a separate DSP processor, multi-channel A/D converter card, multi-channel D/A converter card, digital I/O card, and high-speed counter card. These are housed in a PC bus expansion box, which is in turn connected to a computer [32]. Figure 2.12 shows a dSPACE DS1104 Research & Development (R&D) controller board present at MSU PERL. The D/A channels are labeled DACH1 through DACH8 and A/D channels are labeled ADCH1 through ADCH8.

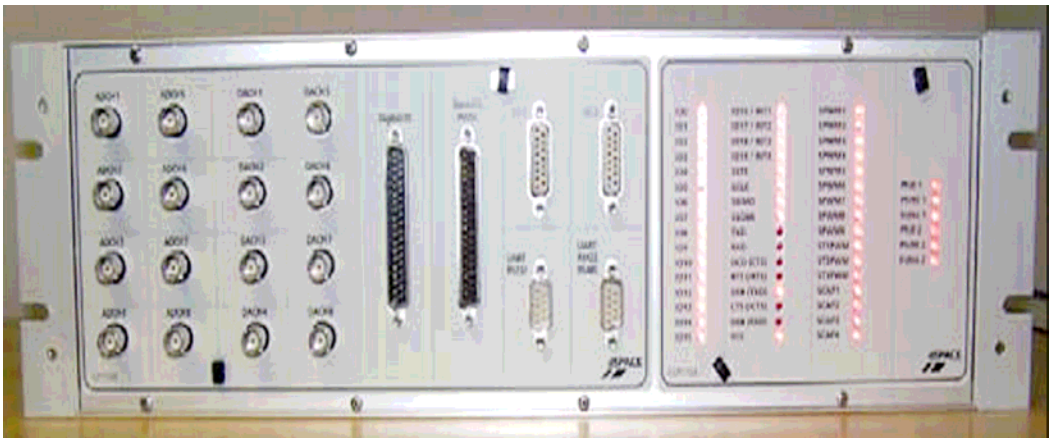


Figure 2.12 dSPACE DS1104 R&D controller board.

The dSPACE software offers an excellent GUI (graphical User Interface) called "Control Desk". This "Control Desk" is used to control and observe signals. It also allows data logging and it can be used as an oscilloscope or a logic analyzer in real-time hardware tests.

The general working procedure with dSPACE is to build /design the model in Matlab/Simulink and convert that model into C code using real-time workshop by the Math Works Inc. This code is downloaded into dSPACE controller to run in real-time [32].

2.5 Summary

In this chapter, an overview of all the major concepts, software and hardware used for this thesis work are presented. Major emphasis is given on HIL test, RTDS, LabVIEW and NI-PXI. In this thesis work, RTDS is used as real-time power system

simulator. LabVIEW is used to model an overcurrent relay and LabVIEW RT to run it in real-time on NI-PXI controller. NI-PXI is also used as a power system simulator by running Matlab/Simulink models on it through the LabVIEW SIT add-on.

CHAPTER III

MODELING OF POWER SYSTEM TEST CASES

3.1 Introduction

This chapter describes the modeling of power system test cases in Matlab/Simulink and RSCAD. A detailed modeling of two-bus, eight-bus and shipboard power systems is presented in Matlab/Simulink software. The procedure to export voltage and current signals from Matlab/Simulink to LabVIEW using Simulation Interface Toolkit (SIT) is described for all the systems. Additionally, an eight-bus power system modeled in RSCAD software is presented. These power system models can be used to perform real-time power system simulations for conducting Hardware-in-the-Loop (HIL) tests.

3.2 Two-bus Power System Modeling

3.2.1 Modeling in Matlab/Simulink

A two-bus power system test case is modeled in Matlab/Simulink (Figure. 3.1).

The two-bus power system specifications are:

- 13.8 kV AC source
- Fault inception logic, circuit breaker

- Step-down (13.8kV/400V) Δ-Y_g transformer
- Transmission line impedance blocks
- 100 KW load at 400V

The generator produces a line-to-line voltage of 13.8 kV. The load is a three phase series RLC load. The transmission line is 100 km long with parameters R=0.028(Ω/km) and X=0.325 (Ω/km).

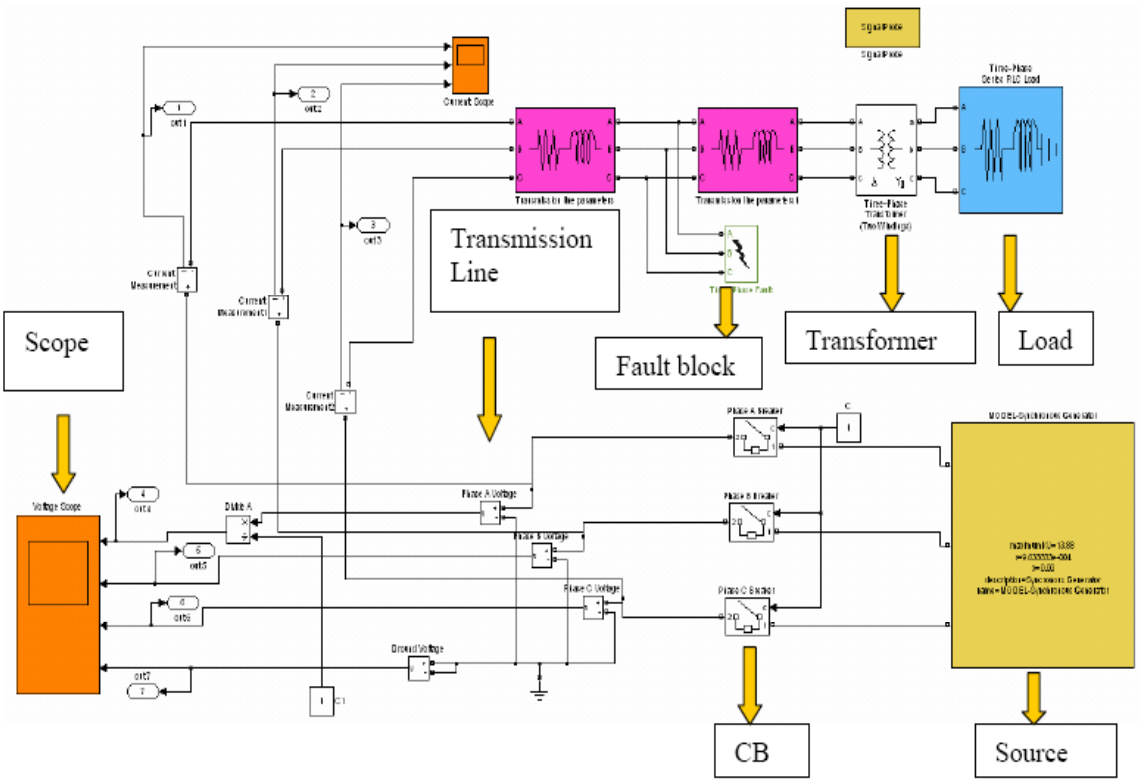


Figure 3.1 Two-bus power system test case in Matlab/Simulink

The fault inception logic is present at 50% of the transmission line length. The circuit breakers are externally controlled and are kept closed by feeding "high" signal

continuously. The signals to control the circuit breakers will be coming from the relay, once the relay model or hardware relay is available. The step-down transformer supplies the required 400V to the load.

3.2.2 Signal Assignments between Matlab/Simulink and LabVIEW

The LabVIEW front panel is used to observe the real-time power system simulations that were running on real-time target NI-PXI. SIT acts as an interface between Matlab/Simulink and LabVIEW to observe the Simulink results in LabVIEW and also to get the signal out on the NI-PXI system. After creating the LabVIEW user interface (front panel), the user has to specify with which Matlab/Simulink model the VI wants to communicate. The SIT connection manager is used for this purpose. The SIT connection manager is launched by browsing to Tools>> SIT connection Manager [30]. Figure 3.2 depicts the process to upload a Matlab/Simulink model to SIT connection manager. After loading the Matlab/Simulink model, the user must indicate which Simulink parameters correspond with which LabVIEW controls and indicators. The SIT connection manager mapping dialog box establishes these relationships [30]. The simulation environment must be local host (i.e. your computer) and the execution port is 6011, default port for SIT. Figure 3.3 presents the mappings of two-bus power system test case in Matlab/Simulink and corresponding LabVIEW user interface. In Figure 3.3, the parameters under "Label" tab correspond to graphs on LabVIEW user interface.

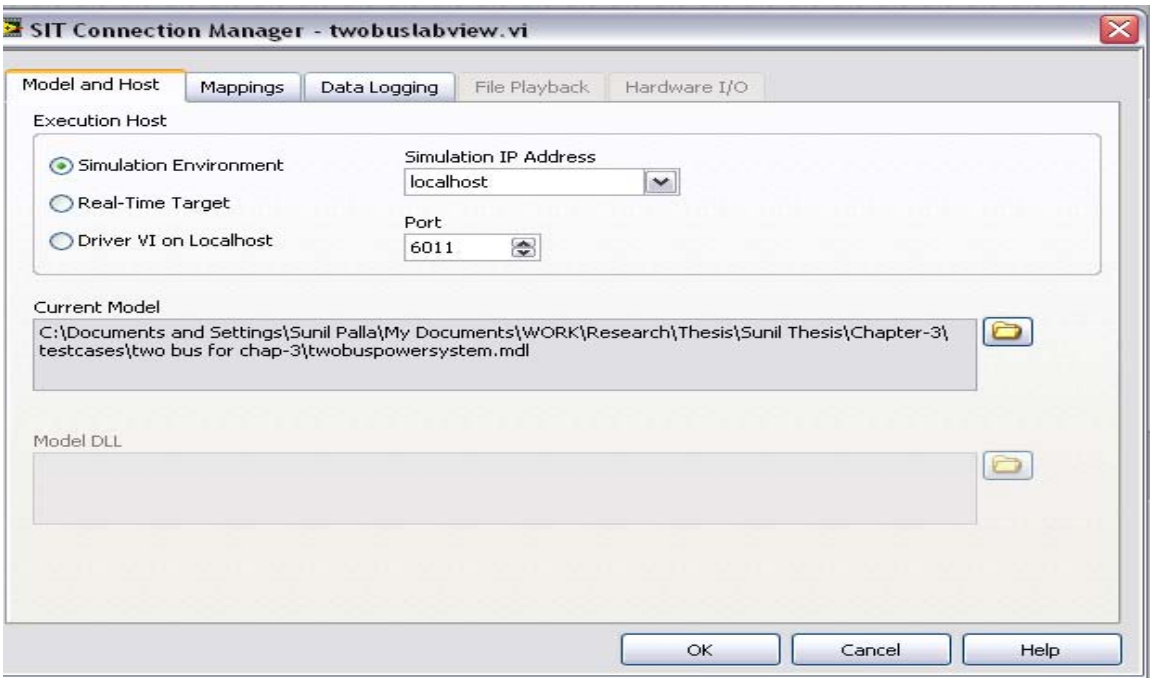


Figure 3.2 Select model dialog box in SIT connection manager.

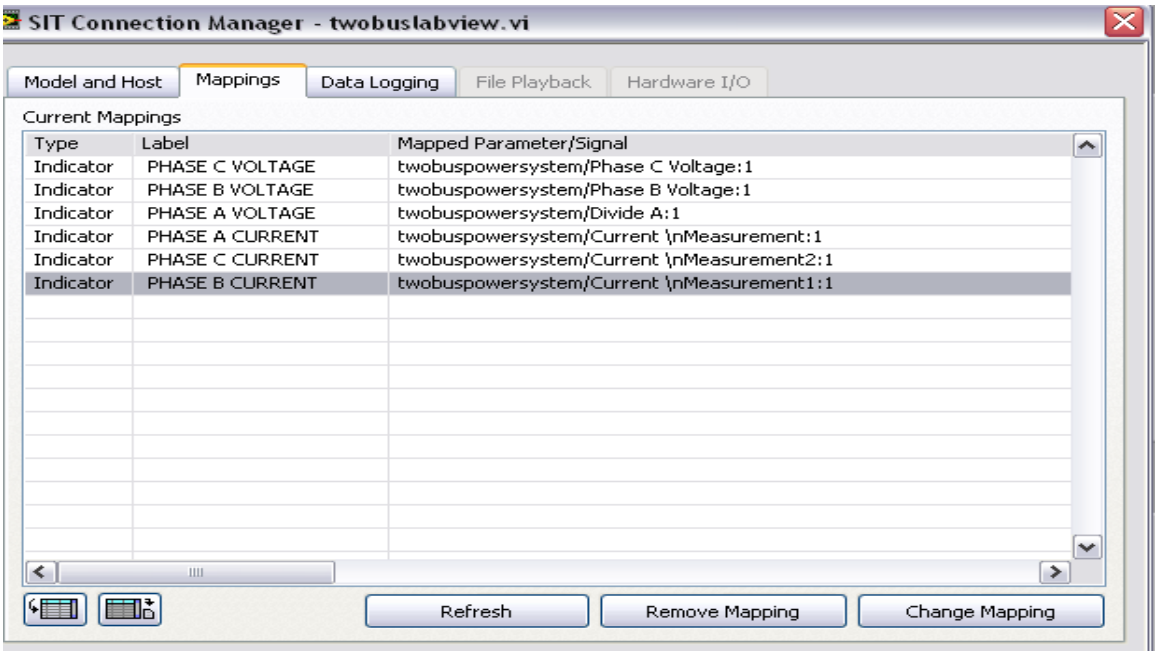


Figure 3.3 Mappings dialog box of SIT connection manager.

The parameters under “Mapped Parameter/Signal” correspond to outports and inports in Matlab/Simulink model. It can be inferred from Figure 3.3 that voltages and currents of a two-bus power system test case are exported to corresponding graphs in LabVIEW.

3.3 Eight-bus Power System Modeling

3.3.1 Modeling in Matlab/Simulink

An eight-bus power system is modeled in Matlab/Simulink (Figure 3.4)

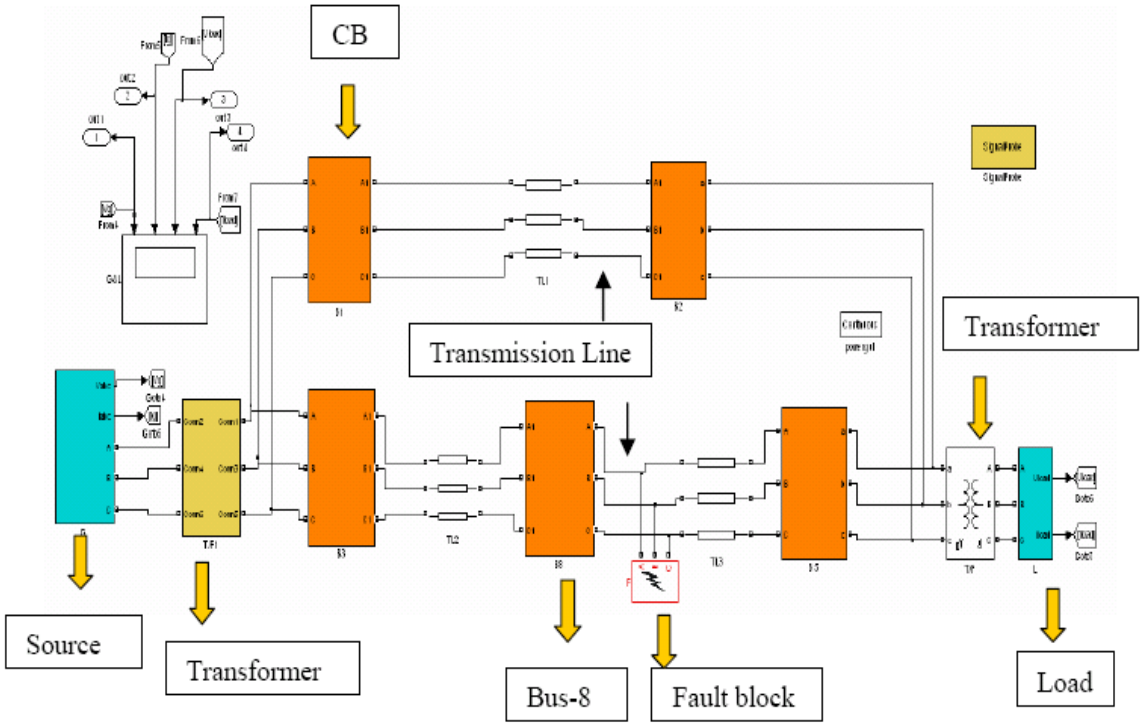


Figure 3.4 Eight-bus power system test case in Matlab/Simulink

The eight-bus power system specifications are:

- 13.8 kV AC source
- Step-up transformer (13.8kV/69kV) – (Δ-Y_g)
- Step-down transformer (69kV/13.8kV)- (Y_{g-} Δ)
- Transmission line impedance blocks
- 100 MW motor load.
- Fault inception block, circuit breakers

This test system has a three-phase source with an angle difference of 120 degrees between each phase and the voltage magnitude is 13.8 kV (phase to phase RMS voltage). There are two parallel transmission lines of 100 km length between the source and load with a line resistance of 0.01273Ω/km, line inductance of 0.9mH/km and the line capacitance is 12.74nF/km. There is a three-phase fault block through which different faults can be placed on the system. There are two transformers, step-up (13.8kV/69kV) near source and step-down (69kV/13.8kV) near load. The three phase current and voltage signals are observed using a scope.

3.3.2 Signal Assignments between Matlab/Simulink and LabVIEW

Figure 3.5 shows the signal mapping of eight-bus system in SIT connection manager. The generator current, load current, generator voltage and load voltage have been mapped to corresponding LabVIEW user interface for eight-bus power system. The execution is done on the host computer itself using SIT on port 6011.

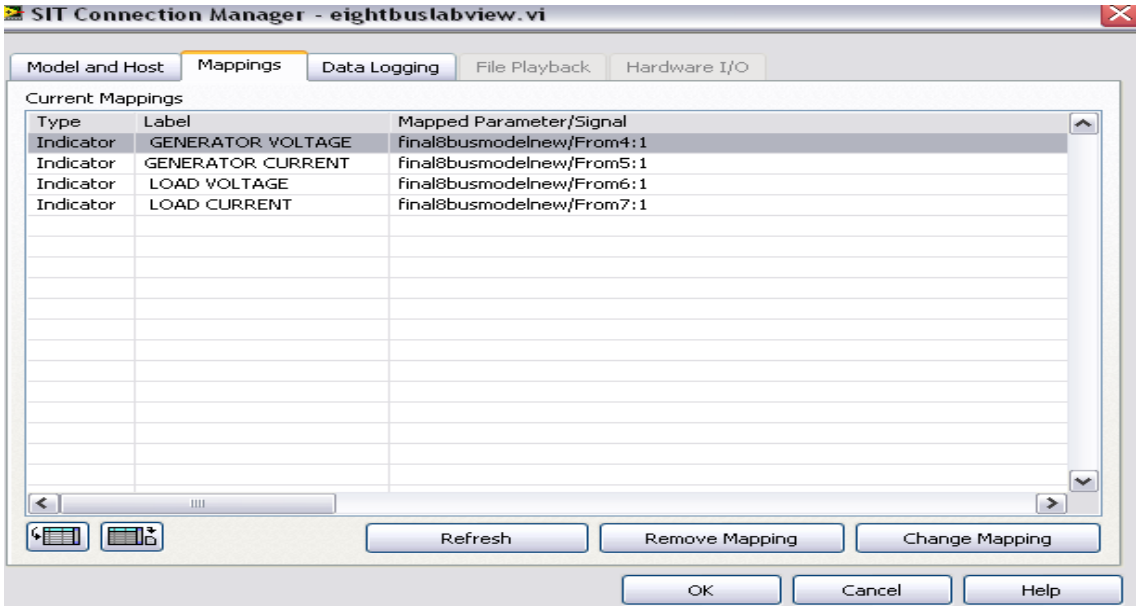


Figure 3.5 Mappings in SIT connection manager for eight-bus power system.

3.4 Shipboard Power System Modeling

3.4.1 Modeling in Matlab/Simulink

A shipboard power system is modeled in Matlab/Simulink (Figure 3.6)

The shipboard power system specifications are:

- 13.8 kV AC source
- Step-down transformer (13.8kV/4.16kV)
- Two 12 MVA motor loads
- Two 5 kW resistive loads.
- Fault inception block, Circuit Breakers (B1 through B16)

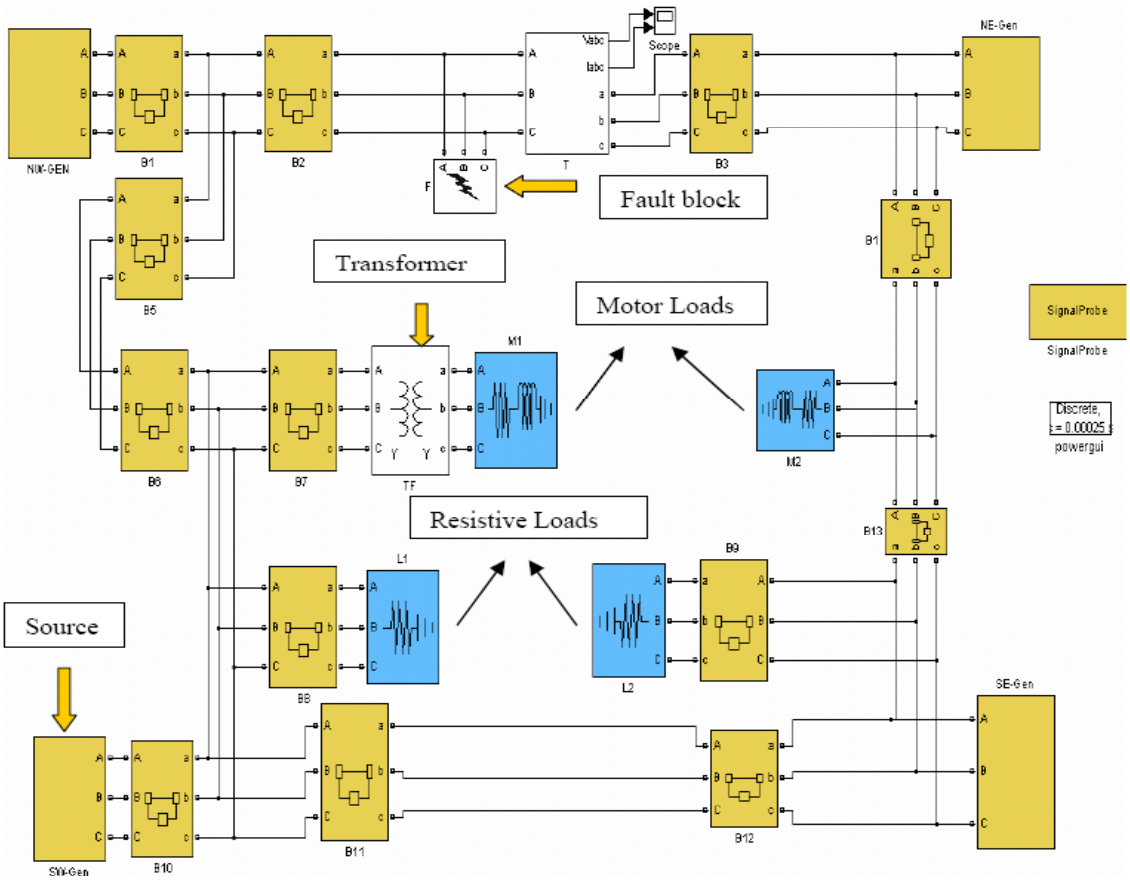


Figure 3.6 Shipboard power system test case in Matlab/Simulink

This shipboard power system has four generators. Northwest, Southwest, Northeast and Southeast generators operate at 13.8 kV. The loads supplied are two induction motors each of 12 MVA and two 5 kW lighting loads. A step-down transformer is used to step down the voltage from 13.8 kV to 4.16 kV to supply a 12 MVA motor (M1). A fault logic block is used in this model also to place faults on the shipboard power system. A total of sixteen (16) circuit breakers are used in the modeling of this test case.

3.4.2 Signal Assignments between Matlab/Simulink and LabVIEW

Figure 3.7 shows the signal mapping of the shipboard power system in SIT connection manager. In this shipboard system, the system currents and voltages at a bus near the fault are of importance.

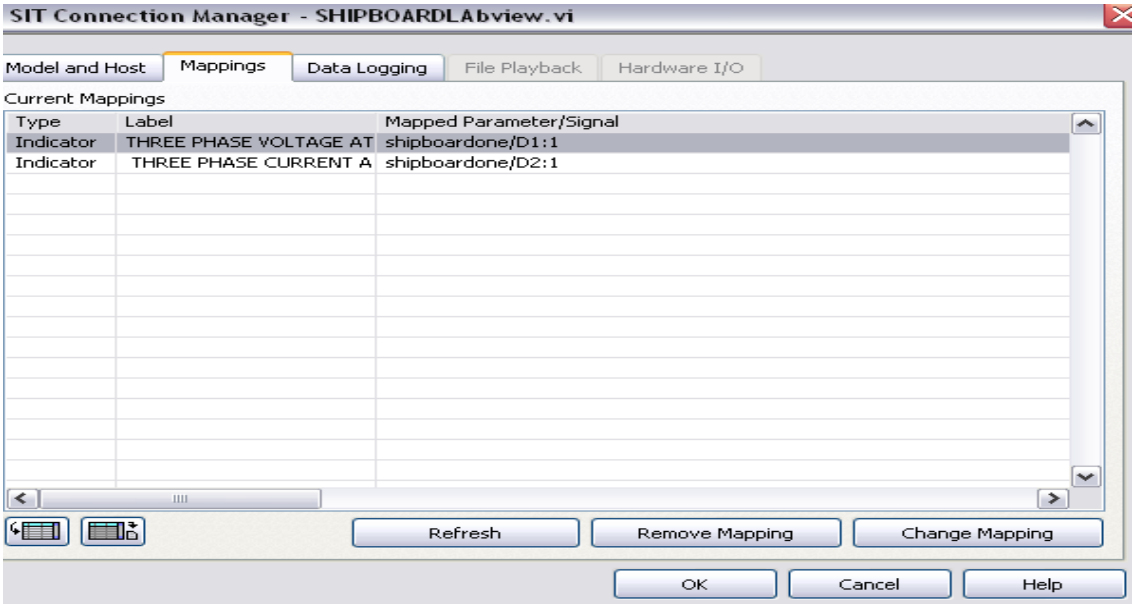


Figure 3.7 Mappings in SIT connection manager for shipboard power system

So the three-phase current and voltage at bus-3 are mapped between the Matlab/Simulink model and LabVIEW model.

3.5 Modeling of Eight-bus Power System in RTDS

The test system developed in RTDS is an 8-bus model in RSCAD (Figure 3.8). The test system has two parallel transmission lines of 100 km length between the source and load. The system specifications are:

- 230kV AC source
- Fault inception logic
- Parallel transmission lines of length 100 km
- Step-down transformer (230kV/15kV) - (Y_{g-} Δ)
- 1200MVA, 15kV synchronous motor
- C.T's, P.T's and circuit breakers

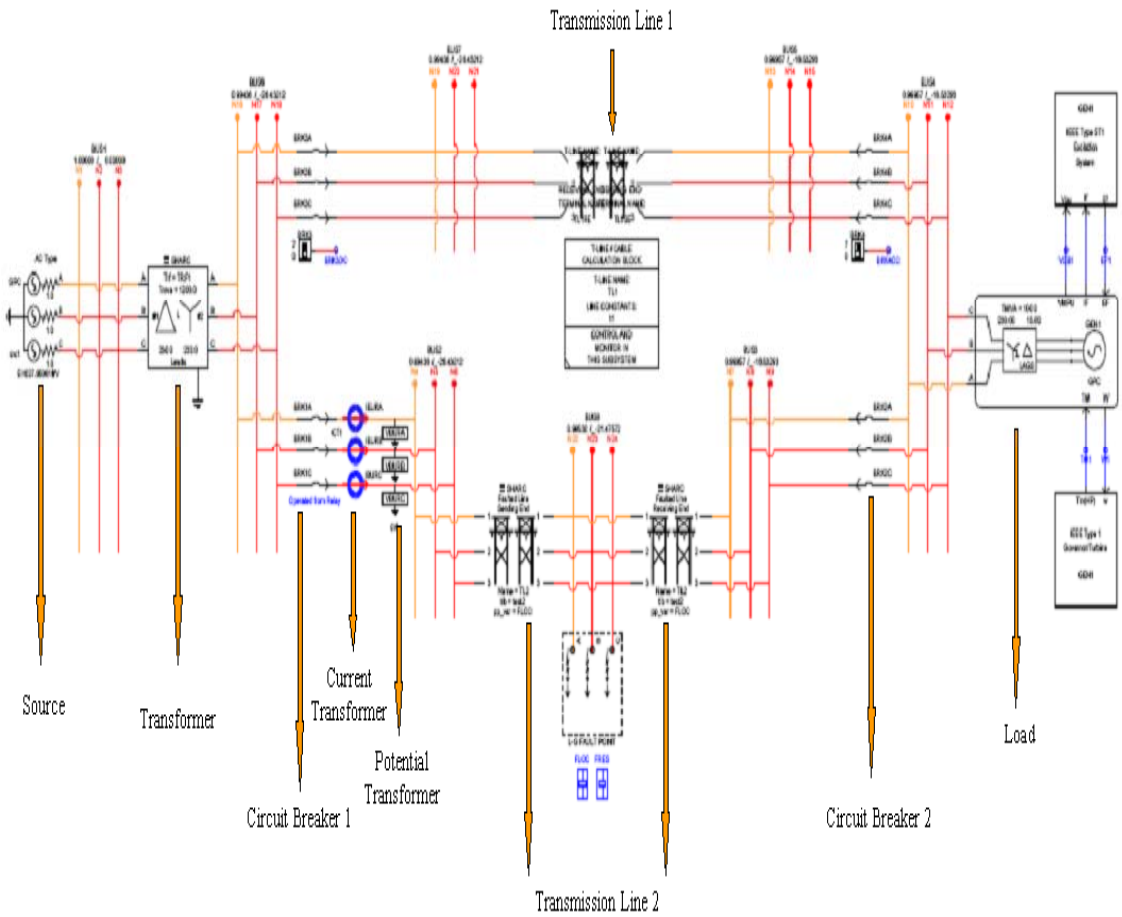


Figure 3.8 Eight-bus power system test case in RSCAD [12]

The transmission lines presented in the test system have been modeled using 'T-Line' module of RSCAD [12]. The load is a synchronous machine in motoring mode. The transformer on the load side is connected to the synchronous machine internally. The fault inception logic is used to put faults into A, B, and C phases of the transmission line. The fault block is placed on bus-8, which is at 50% length of the transmission line. The CT ratio of the current transformer is 300:1. The CT and PT are modeled in detail to reflect more realistic characteristics.

3.6 Summary

Modeling of two-bus, eight-bus and shipboard power systems in Matlab/Simulink has been presented in this chapter. The procedure to assign voltage and current signals of the Matlab/Simulink power system models to corresponding LabVIEW user interface is described. Modeling of eight-bus power system in RSCAD is also presented. The RSCAD model and the Matlab/Simulink models are used to conduct HIL tests for comparative study in this research work.

CHAPTER IV

MODELING OF PROTECTIVE OVERCURRENT RELAY

4.1 Introduction

This chapter presents the development of Matlab/Simulink and LabVIEW overcurrent relay models. Simple logic for overcurrent relay protection has been presented in section 4.2. In-depth explanation of each building block of Matlab/Simulink and LabVIEW relay model is presented. Further, the different modes of operation of the relay model are presented. The procedure followed to run the relay model in real-time on a remote target is explained. Results obtained by running the relay model on the NI-PXI target are also presented. This chapter also presents a flow chart, which explains the algorithm behind the relay modeling and its operation.

4.2 Overcurrent Relay Overview

The aim of protective relays is to detect abnormal conditions or defective equipment, initiate actions to disconnect faulted parts of the system and minimize the impact on remaining parts of the system [3]. The final objective is protecting the power system from detrimental power system conditions. High currents, over/under voltages,

and over/under frequency are examples of these conditions. The over-current relay makes use of the system current (peak value or RMS value) to detect the fault [9].

To clearly illustrate the simple over-current relay logic, consider I_{sys} as the system current magnitude. Assume I_{th} as the threshold current magnitude. Threshold current or pick-up current can be defined as the minimum current needed to cause the relay to trip the circuit. If

$|I_{sys}| < |I_{th}|$ Over-current relay does not gives trip signal

$|I_{sys}| \geq |I_{th}|$ Over-current relay gives a trip signal [9]

In most instances of a fault, the current level increases significantly from its pre-fault value and the over-current relay picks this abnormal situation. A relay can also perform other necessary analysis/action additionally.

4.3 Modeling of Overcurrent Relay in Matlab/Simulink

The Matlab/Simulink over-current relay model presented here is used as a basis for development of LabVIEW relay model. This Matlab/Simulink relay model, shown in Figure 4.1 is taken from reference [9]. The relay model is divided into three parts for clear understanding.

PART A: This part is for analog to digital conversion. Iabc_Relay1 is the fault current drawn from power system. CTR_T1 is the current transformer (CT) ratio (3000:5 = 600). Product block is used (Iabc_Relay1/ CTR_T1) to step-down the current. An Ideal sampler and Zero- Order hold (ZOH) gives the required analog to digital conversion. The

ZOH circuit acts as a sample and hold circuit. Sampling is done at the rate of 16 samples/cycle of the waveform.

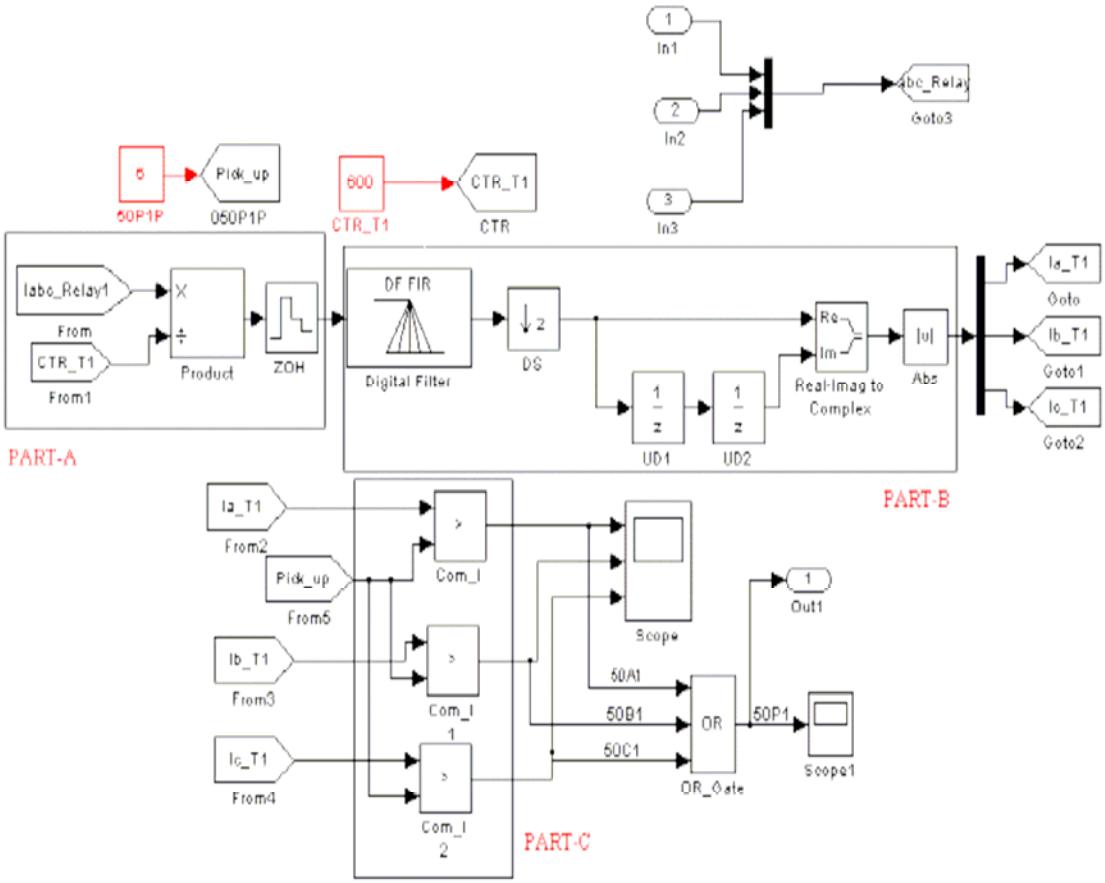


Figure 4.1 Overcurrent Relay model in Matlab/Simulink [9]

PART B: This part is for filtering and phasor calculation. A digital filter (finite impulse response) is used to obtain the fundamental signal. To reduce the sampling rate, a down sampling block is used. The down sampling block is necessary to have an anti-aliasing effect. Anti-aliasing can be defined as the procedure to restore the original shape of the fundamental i.e. sine wave. After down sampling, the resultant current signal is fed to

"Real-Imag to Complex" block. The output of complex block is passed through the "Abs" block to get the magnitude of current signal, which gives the current to be compared with pickup value.

PART C: The currents obtained in Part B are compared with pick up value for all the three phases and the required trip signal is obtained. In this model, the pick-up value is set to 6 times the rated secondary current of CT. For example under normal operation, sec current of the CT is 5A. If the current goes beyond 5*6=30A then the relay gives a trip/reclose signal. Scope1 gives us the result of an 'OR' function on all the three-trip/reclose outputs from phases A, B, C [9].

The Matlab/Simulink instantaneous overcurrent relay model is simple. It has its own drawbacks such as there are no separate signals for trip and reclose, poor performance for higher order systems, and no additional functionality of relay except the basic overcurrent logic. There is a certain need of development in this area. This has been improved by development of a LabVIEW relay that can run in non-real-time as well as real-time. The LabVIEW relay has additional functionality apart from basic overcurrent logic.

4.4 Modeling of Overcurrent Relay in LabVIEW Software

4.4.1 Introduction

This section of the chapter describes the methodology to develop the overcurrent relay model in LabVIEW. Figure 4.2 shows the general diagram of functionality of

instantaneous overcurrent relay. The secondary CT current is filtered using an analog filter. Further, it is converted to digital signals using analog to digital converter (ADC).

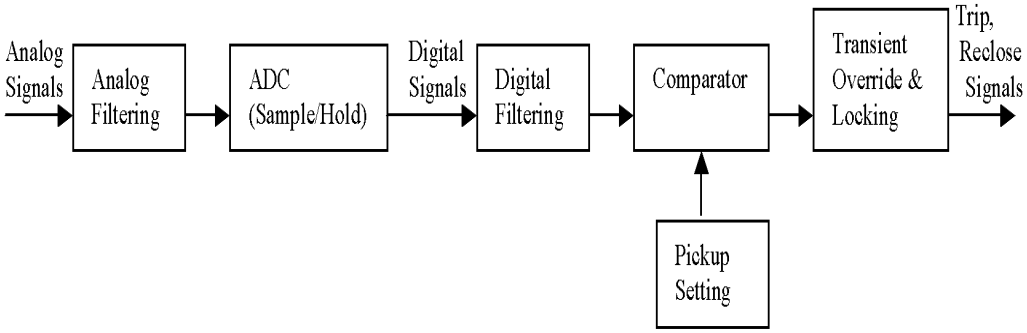


Figure 4.2 Design of overcurrent relay

The output of the ADC is again filtered using digital filter. The output of digital filter is compared to the threshold value and the corresponding trip and reclose signals are given if there is a fault. Each building block of the LabVIEW relay model, as shown in Figure 4.2 is explained in sub-sections 4.4.2 through 4.4.5.

4.4.2 Analog to Digital Converter

An Analog to Digital converter (ADC) plays a vital role in digital relay design. An ADC converts the acquired analog three phase current signal into digital form. An ADC is implemented by using a ZOH device. A ZOH block is used in modeling for converting the analog signal into a digital signal [9], [33]. In LabVIEW relay modeling, the ZOH device samples the signal at the rate of 16 samples/cycle. An ideal sampler and ZOH are equivalent to an ADC unit.

4.4.3 Filtering

Before conversion of the acquired analog three phase current signal into digital form, the signal should be filtered. Analog signals may have high noise levels and are filtered using an analog filter. In LabVIEW relay modeling, a 5th order band pass Butterworth filter with band pass frequency ranging from 40 to 80Hz is used for filtering purposes. Even though a Butterworth filter has a slower roll-off at lower orders, it has more linear phase response in the pass band than the Chebyshev Type I/Type II and elliptic filters [34]. The digital filter is a very important part in microprocessor based digital relays. In this LabVIEW relay model, a low pass digital FIR filter is used [35]. The analog filter performs well to remove noise levels from the analog input signals and the digital filter further makes sure to get smoother signal.

4.4.4 Comparator and Pick-up

After digital filtering, the signals are passed through a comparator. The comparator compares the peak values of the signal against the threshold value. The threshold should be set at a level so that it is above the maximum load current at peak load situations [36]. The normal steady state three-phase current coming from the RSCAD power system model (Figure 3.11) at bus-8 is 6A peak-peak (p-p) at the CT secondary side. In the LabVIEW overcurrent relay model, the threshold is set at 12Ap-p, well above the normal operating current range of 6Ap-p. When the fault current is above the threshold, the model issues a digital trip signal to open the system. After the user defined time period, it issues the reclose signal to close the system.

4.4.5 Transient override and Locking

Apart from the normal instantaneous operation of the overcurrent relay, the relay model consists of two more features. They are transient override and locking features. Transient override is a feature, where the operator can set the relay to ignore switching transients on the system that cause high peak currents in short periods of time. This feature is also useful in coordinating a relay with other relays in a system by introducing a delay. In the relay model, there is a numeric control. If the operator selects a number in the numeric control, the model ignores that number of fault cycles and does not give a trip or reclose signal.

Locking is another feature where the relay locks itself for severe faults. For example, if a fault occurs on the system, the relay model performs its trip and a reclose action. If the fault is still there, it again performs a trip and reclose action. If the fault is still there on the system up to 60 cycles (this number can be set at user defined value), then the model assumes it as a severe fault. The model locks out and trips the system. At this stage, the "Lock" button provided on the model glows red showing that the relay is locked. After the fault is cleared, the operator has to reclose the system by pressing the "Lock-Release" button provided on the model. Then the system recloses and returns to its normal operation.

4.5 Modes of Operation

LabVIEW relay model can be operated in two modes of operation.

4.5.1 Internal Mode of operation

In this mode of operation, the user can test the model for proper operation. The current signals that need to be monitored are provided by signal sources. Three single phase sources are used with a 120 degrees phase shift to form a three-phase signal. The three-phase signal has a peak value of 3000A. The CT ratio is 1600:1 (Theoretical testing purpose).

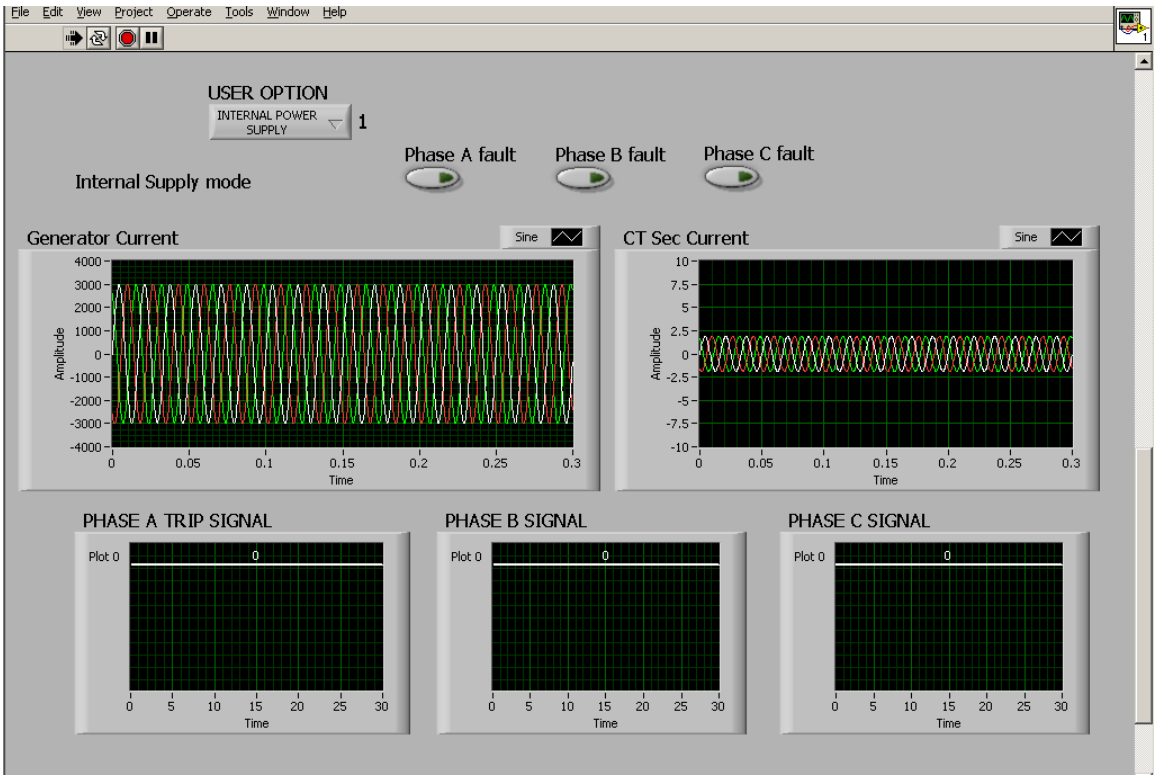


Figure 4.3 Internal mode of operation for LabVIEW relay

Figure 4.3 shows the front panel of LabVIEW relay model in internal mode of operation. Options are provided to place faults on the system. Simulations of the relay model for different faults in internal mode are provided in Chapter VI.

4.5.2 External Mode of operation

External mode of operation of the relay model reveals the real-time operating capability of the model. In this mode of operation, the model runs in real-time on a remote target getting the current signals from power system simulators such as RTDS. A detailed explanation of a relay model in external mode of operation is presented in sections 4.6 and 4.7. Several HIL tests are conducted with the relay model running in external mode. The results of those tests are provided in Chapter VI.

4.6 Real-Time Performance of LabVIEW Overcurrent Relay Model

4.6.1 Creating a real-time project to run the LabVIEW VI

In order to run a LabVIEW VI in real time on a real-time target, a real-time project has to be created. A real time target can be a NI-PXI, Compact Field Point or a Compact RIO. While creating the project, it runs through the option of adding a real-time target. The target, NI-PXI system is added in this case. After the project is created, the NI-PXI should be connected and the required VI is deployed into the NI-PXI for running in real-time. In this case, the LabVIEW overcurrent relay model is deployed into the NI-PXI-8196 controller.

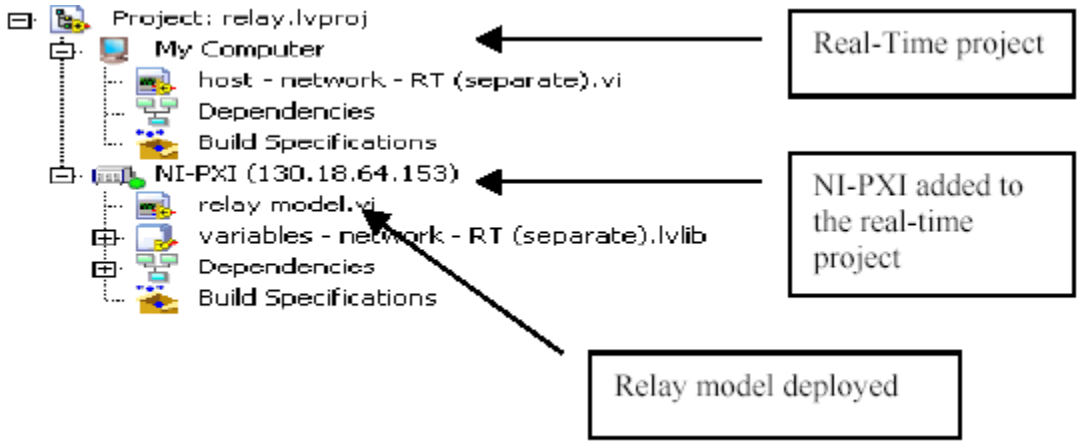


Figure 4.4 LabVIEW Real-time project window

Figure 4.4 shows a screenshot of real-time project window. For clarity purposes the original screenshot is modified. Figure 4.4 depicts that the NI-PXI device is connected and it is ready for any VI deployment. Further, it also shows that the relay model is deployed and running on NI-PXI in real-time.

4.6.2 Analog and Digital I/O

An overcurrent relay needs a three-phase system current as its input. The three phase currents in the power system are step-downed using a current transformer with a required CT ratio and provided to the overcurrent relay. In the case of LabVIEW relay modeling, RTDS provides the three phase currents. These system currents are at bus-8 in the power system (Figure 3.11) and are step-downed using a current transformer with a CT ratio of 300:1. Analog channels of NI PXI 6251 collect these signals with a sampling rate of 600 samples/sec.

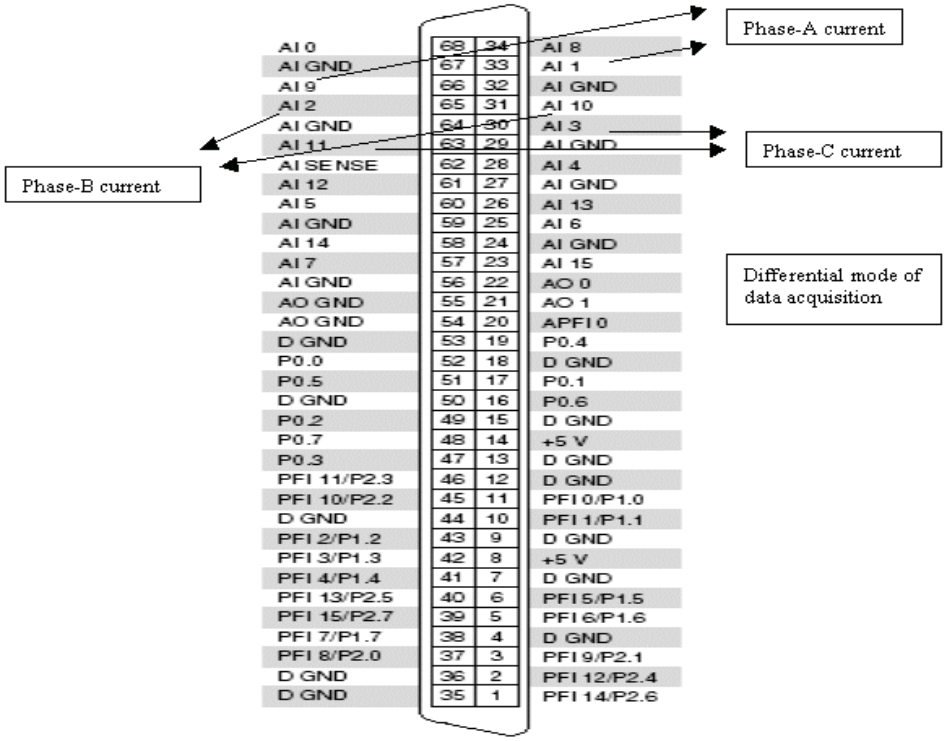


Figure 4.5 Pin out for NI-PXI 6251 [37]

Figure 4.5 presents the pin-out of NI-PXI 6251 device and the way phase currents are collected from RTDS. Analog channels are used in differential configuration mode for best possible signal acquisition and the combinations used are AI1 and AI9 for phase-A current, AI2 and AI10 for phase-B current, AI3 and AI11 for phase-C current. The NI PXI-6608 is a high precision counter/timer with digital I/O. The digital trip and reclose signals are generated using NI PXI-6608 from channels P0.1 through P0.6. Figure 4.6 depicts the way digital trip and reclose signals are routed to RTDS from NI-PXI 6608.

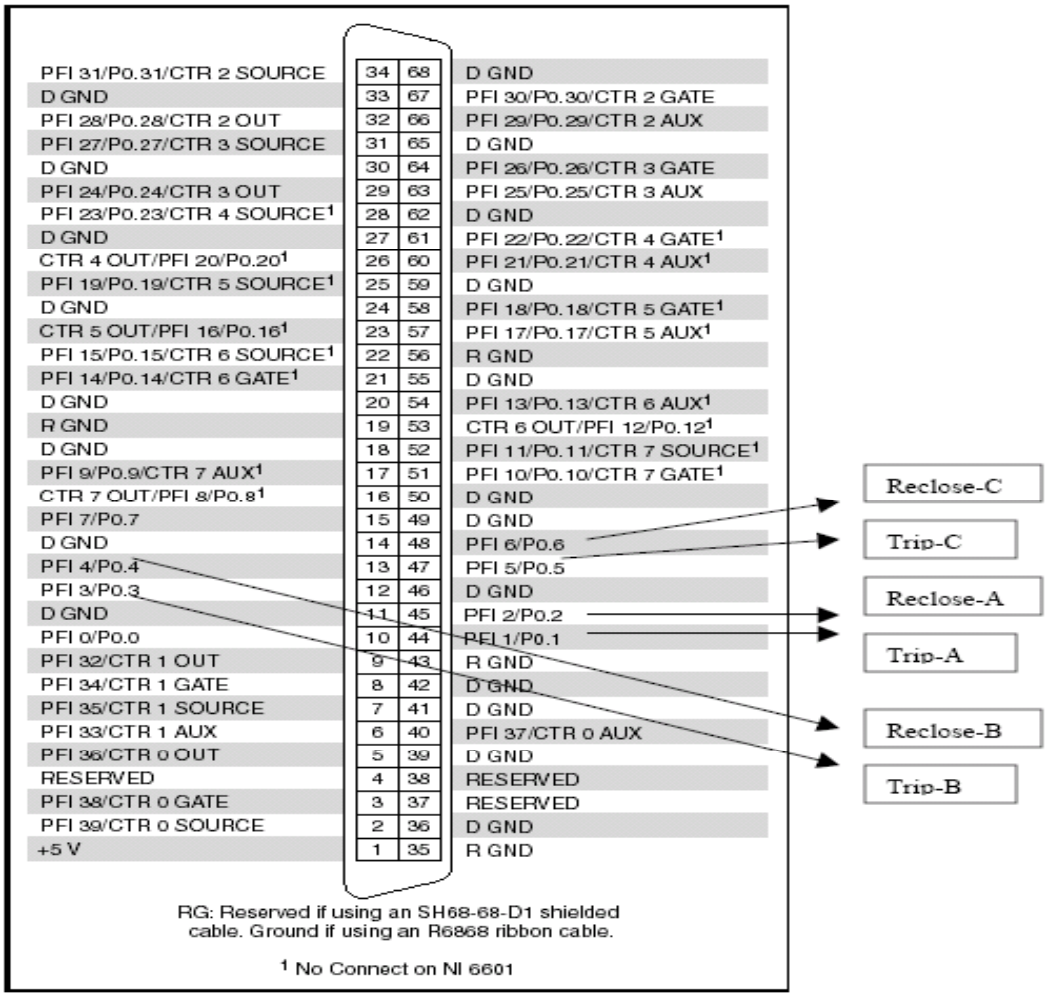


Figure 4.6 Pin out for NI-PXI 6608 [38]

4.6.3 Front Panel View of Overcurrent Relay in LabVIEW RT

Figure 4.7 is the front panel of relay model. The code for the relay model resides in its block diagram. In this front panel, the operator can see the secondary current of CT, fault indicators, trip signals and reclose signals. In addition, transient override and

locking can also be seen in Figure 4.7. The CT secondary currents are scaled to make sure that the currents are within the ranges of NI PXI data acquisition cards.

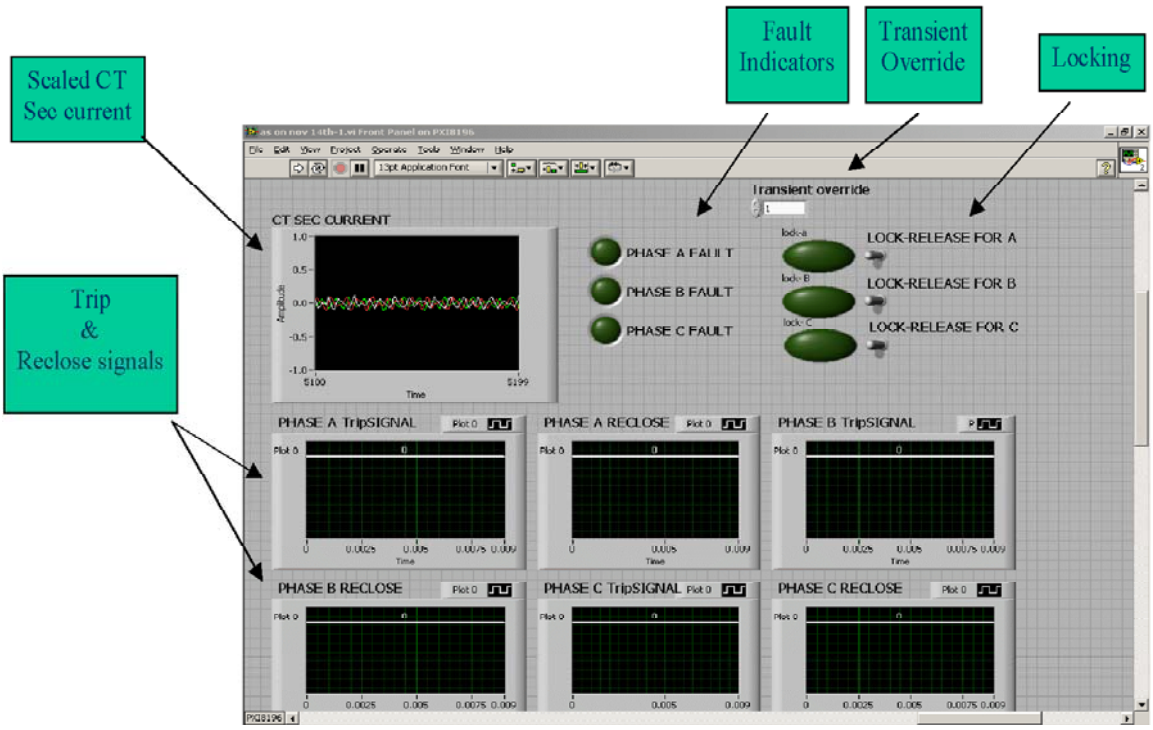


Figure 4.7 Front panel of LabVIEW Overcurrent Relay

Figure 4.8 shows a single phase-A to ground fault on the system. For the phase-A fault, the fault indicator glows and the corresponding trip signal is generated.

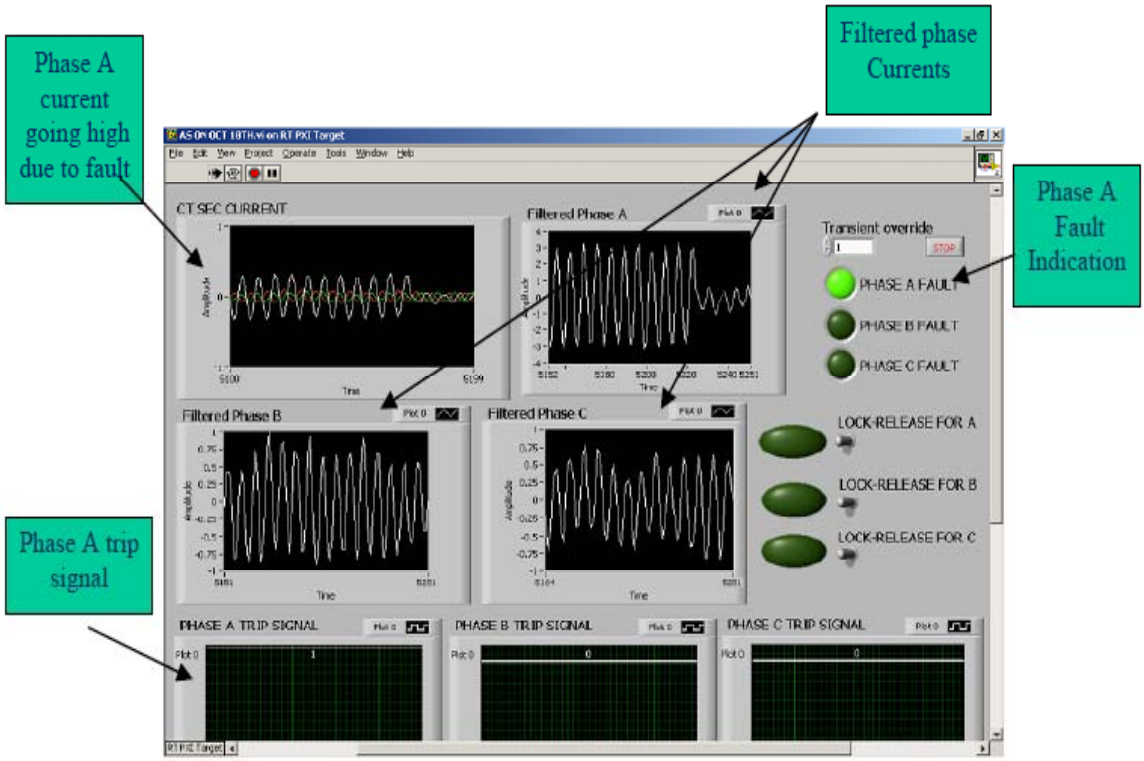


Figure 4.8 Relay model showing Phase-A fault

4.7 Real-Time Operational Logic for the Relay Model

The functionality of the instantaneous/time delay overcurrent relay model in real-time is shown in Figure 4.9. As soon as the relay model starts running, it first initializes the variables count, trip, reclose, lock and N to zero. The variable N represents the transient override, explained in section 4.4.4. Assume the value of N = 1. The DAQ cards sample the current signals. The sampled three-phase signals are split into three single-phase current signals. Each signal is compared to the threshold value. If there is a fault, sampled signal will be greater than threshold value and then the count is incremented by 1. If the sampled signal is less than the threshold value then there is no increment in count

and its value stays at zero. The next step is to check the count value with N+ 16. In this example, this occurs to be 1+ 16 = 17. (Each cycle is sampled at the rate of 16 samples/cycle by the zero order hold circuit).

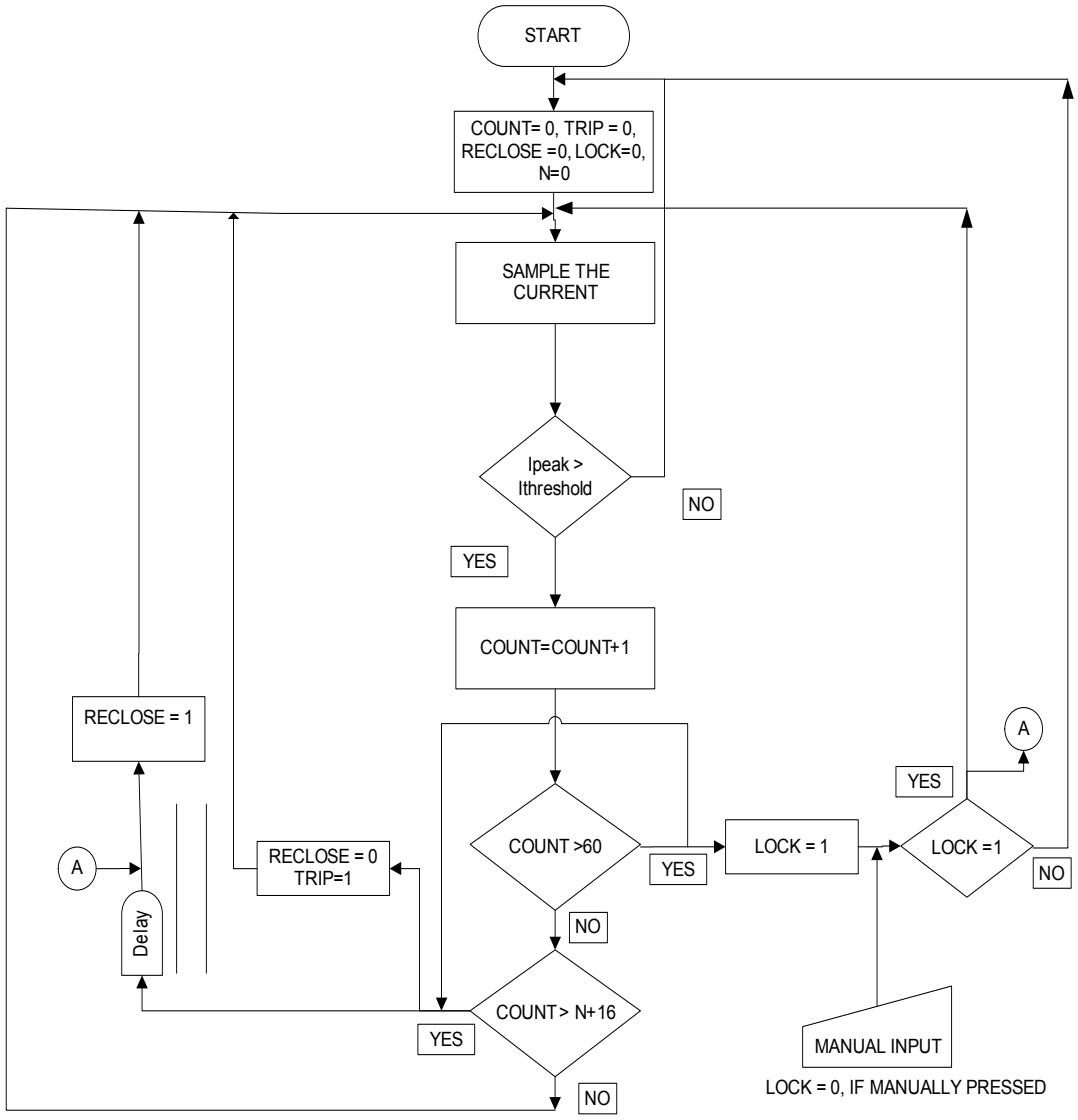


Figure 4.9 Flowchart showing the functionality of relay model

If the count is greater than 17, then the relay model trips the system (i.e.) the fault is present for more than 1 cycle in this case and it is not as a transient. After user defined cycles, the model issues a reclose signal. The process continues again for sampling, comparing, counting and giving a trip and reclose. Even after multiple trips and recloses if the fault still exists, then it can be considered as a severe fault. In this model, the fault is considered to be severe, if it exists for 60 (user defined) continuous cycles. In this case, the relay locks by giving a trip and there after opens the system. At this moment, the relay model waits for the manual input from the operator to reclose the system. The system will be returned to normal operation once the operator clears the fault and clicks on the lock release button.

4.8 Advantages of LabVIEW Relay Model

The LabVIEW design platform is a very flexible design platform to design virtual instruments. The express VI'S, functions etc gives its user the required design freedom. LabVIEW overcurrent relay model is very flexible in terms of its functionality. For example, the transient override is user defined. Using this feature, the relay can be made to ignore as many fault cycles as possible. This feature can also be helpful in introducing intentional delay making the relay model to work as time-delay overcurrent relay. Apart from this, this transient override feature can be helpful in tuning the relay model for coordination functions. The locking feature is another important feature useful to protect the system from severe faults. Another main advantage of the LabVIEW relay model is that it can test its performance on its own by using its internal model of operation.

4.9 Summary

This chapter gives a detailed description of overcurrent relay modeling in Matlab/Simulink and LabVIEW software. Details of essential building blocks such as, filters, and ADC are discussed for both the models. Different modes of operation of the relay model are also presented. In section 4.5, the procedure followed to run the relay model in real-time is explained. The front panel views of overcurrent relay model are shown under no-fault condition and single phase to ground fault condition. The algorithm followed to develop the relay model is also presented. The advantages of LabVIEW relay model are also explained. This overcurrent relay model can provide a first order approximation for a commercial overcurrent relay. The developed model can be useful for HIL testing, where cost and time implications come into effect.

CHAPTER V

SIMULATION RESULTS FOR DEVELOPED SOFTWARE MODELS

5.1 Introduction

Simulating the Matlab/Simulink power system test cases under no-fault condition helps to study their steady state performances. This chapter presents those simulations. The screen shots of results are taken from Matlab/Simulink environment. The corresponding LabVIEW user interface results of the test cases are presented. Performance of the overcurrent relay model developed in Matlab/Simulink, explained in Chapter IV is also presented. Later on, this chapter evaluates the performance of the relay model for different kinds of faults on different power system test cases.

5.2 No-Fault Simulation Results in Matlab/Simulink and LabVIEW

5.2.1 Two-bus Power System Test Case

5.2.1.1 Simulation for No-Fault condition in Matlab/Simulink

The Matlab/Simulink two-bus power system test case shown in Chapter III, Figure 3.1 is simulated under no-fault condition. Figure 5.1 shows the three phase voltages and the ground voltage of the system at no-fault condition. The phase voltages are at 12 kVrms approximately and ground voltage is at 0 V.

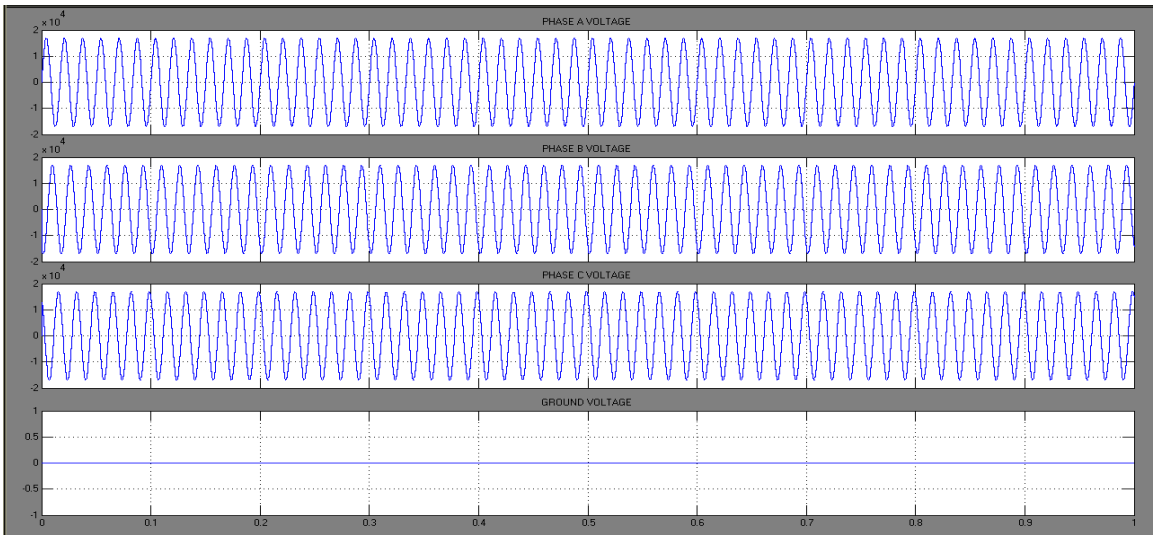


Figure 5.1 Phase voltages of the two-bus power system test case

Figure 5.2 depicts the three single-phase currents of the two-bus system at no-fault condition. The phase currents are at $7A_{p\text{-}p}$.

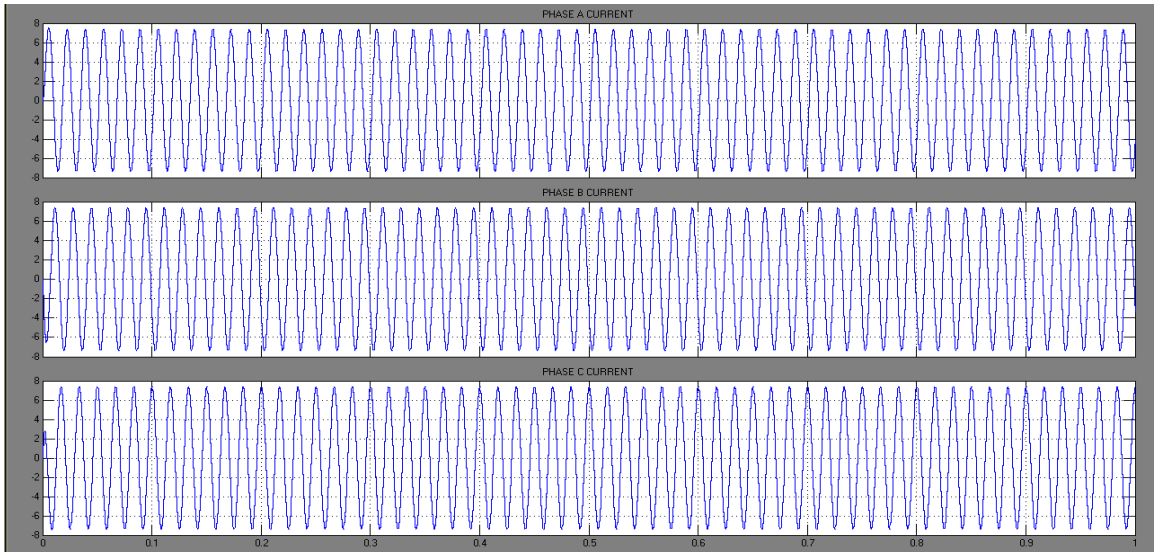


Figure 5.2 Phase currents of the two-bus power system model

5.2.1.2 *LabVIEW User Interface*

The LabVIEW user interface is the front panel of the LabVIEW VI, where the user can observe the output. This front panel of the LabVIEW VI contains graphs for phase voltages and currents. This block diagram code initializes the simulation, sets the parameter values, and receives the indicator updates from the Simulink model to interact with the model DLL. Figure 5.3 shows the LabVIEW User Interface for phase currents and phase voltages. The phase currents and voltages in LabVIEW user interface match with those of in figures 5.1 and 5.2.

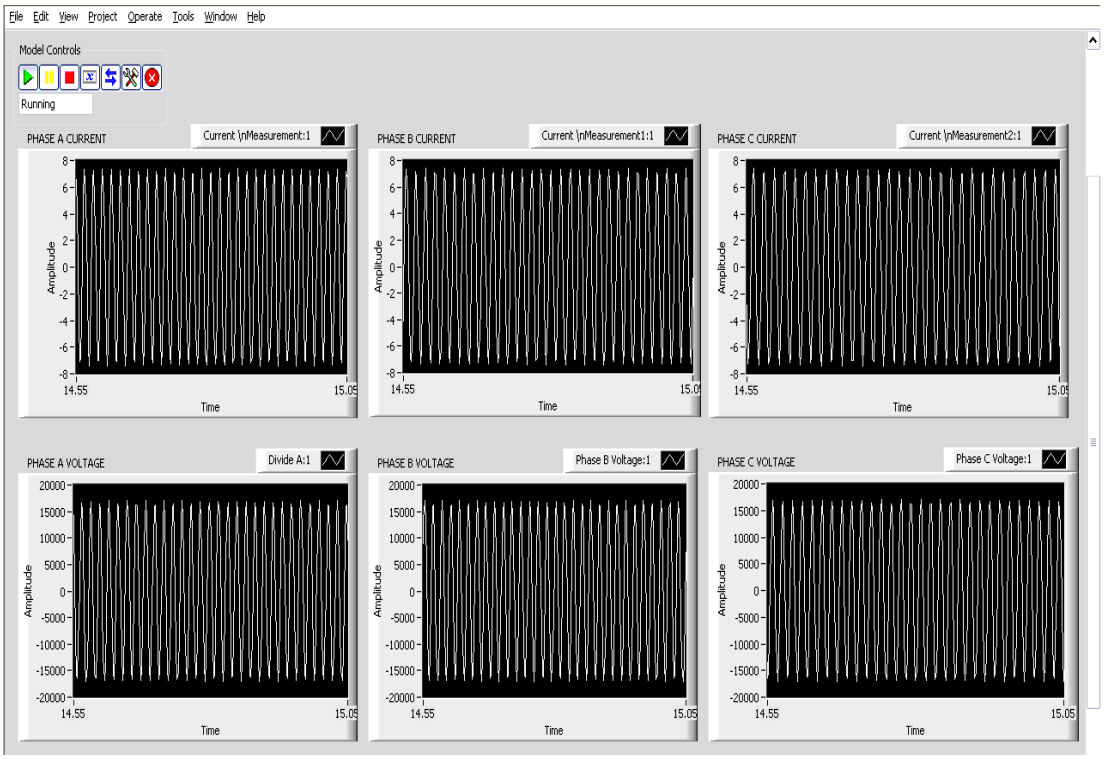


Figure 5.3 LabVIEW User Interface for the two-bus power system model

5.2.2 Eight-bus Power System Test Case

The Matlab/Simulink eight-bus power system test case shown in Chapter III, Figure 3.5 is simulated under no-fault condition. The three-phase generator voltage, three-phase generator current, three-phase load voltage and three-phase load current, are 9000 Vpeak, 248 Arms, 1344 Vrms, and 71 Arms respectively. The LabVIEW user interface for the eight-bus system depicts the three phase voltages and currents at generator and load. The execution is done on the host computer itself using SIT on port 6011. The generator voltage, current as well as load voltage and current are routed to outports on Matlab/Simulink model and these outports are mapped to the corresponding graphs on the LabVIEW VI. The phase currents and voltages in LabVIEW user interface match with the Matlab/Simulink results.

5.2.3 Shipboard Power System Test Case

The Matlab/Simulink SPS test case shown in Chapter III, Figure 3.8 is simulated under no-fault condition. The three-phase voltages and currents at bus-3 of the shipboard power system are 8100 Vpeak, 70 A respectively. The LabVIEW user interface of SPS also depicts the same as Matlab/Simulink results.

5.3 Software-in-the-Loop Test

Software-in-the-Loop (SIL) test is conducted to test the performance of Matlab/Simulink overcurrent relay model mentioned in Chapter IV. The power system

test cases used for conducting the SIL test are explained in detail in Chapter III. The entire set-up for the SIL testing will be in Matlab/Simulink environment.

5.3.1 Testing with Two-bus power system

SIL test is conducted between the two-bus terrestrial power system and the Matlab/Simulink overcurrent relay model mentioned in Chapter IV. The two-bus model mentioned in Chapter III (Figure 3.1) is modified slightly. The generation has been increased to 500kV line-to-line voltage. The transmission line length and the parameters R and X are kept the same. The real power component of the load is 300MW and reactive power component is 100MVAR. This modification is necessary for future comparison of these results with that of closed loop test results between VTB-RT, running the power system and dSPACE, running overcurrent relay model. The set-up for SIL test between the two-bus terrestrial power system and the relay model is shown in Figure 5.4. The trip/reclose signal coming from the instantaneous overcurrent relay model is boolean in nature. The circuit breaker present in the power system accepts either “0” or “1”. Therefore a data type conversion block is placed to covert the data coming from relay model to circuit breaker.

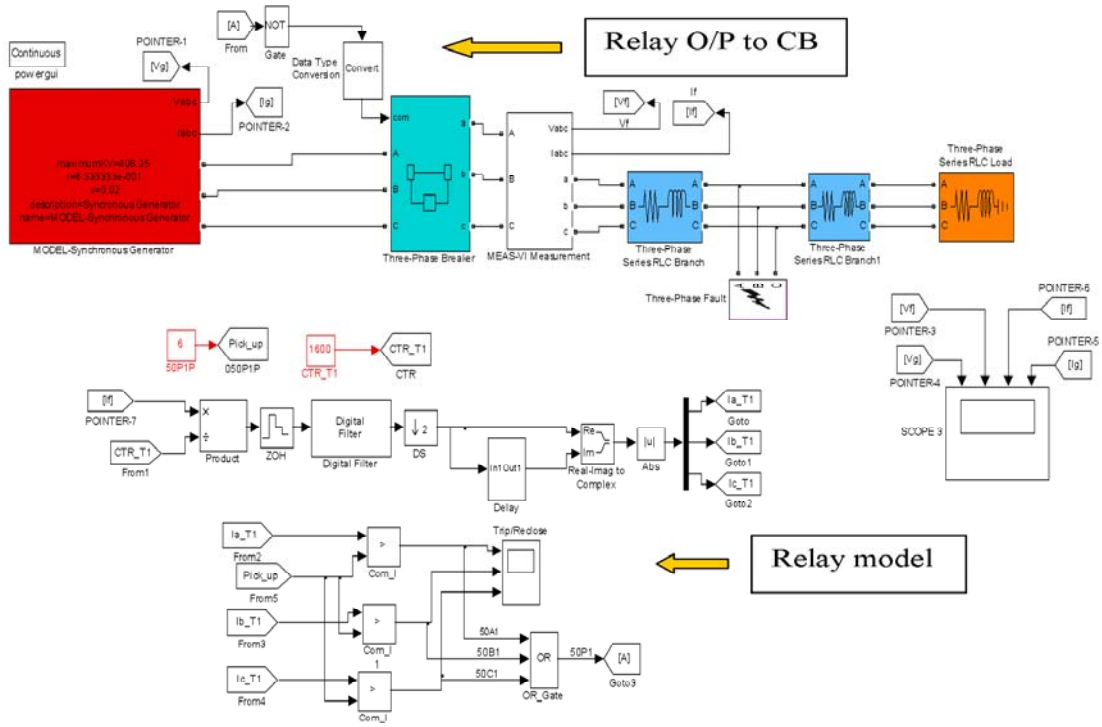


Figure 5.4 SIL test with two-bus power system and relay model

Figure 5.5 shows the results for SIL test between two-bus power system and relay model for L-G fault on phase-A. The results shown in Figure 5.5 depict generator voltage, line voltage, generator current and line current. Phase-A to ground fault is injected into the system from 0.2 to 0.25 secs. The CT ratio is 1600:1 and the pick up current is 6 times the normal value. The relay model recognizes the fault within half of a cycle and trips the system. The system is reclosed at 0.25 secs. Figure 5.6 shows the trip/reclose signal generated by relay model for L-G fault on phase-A.

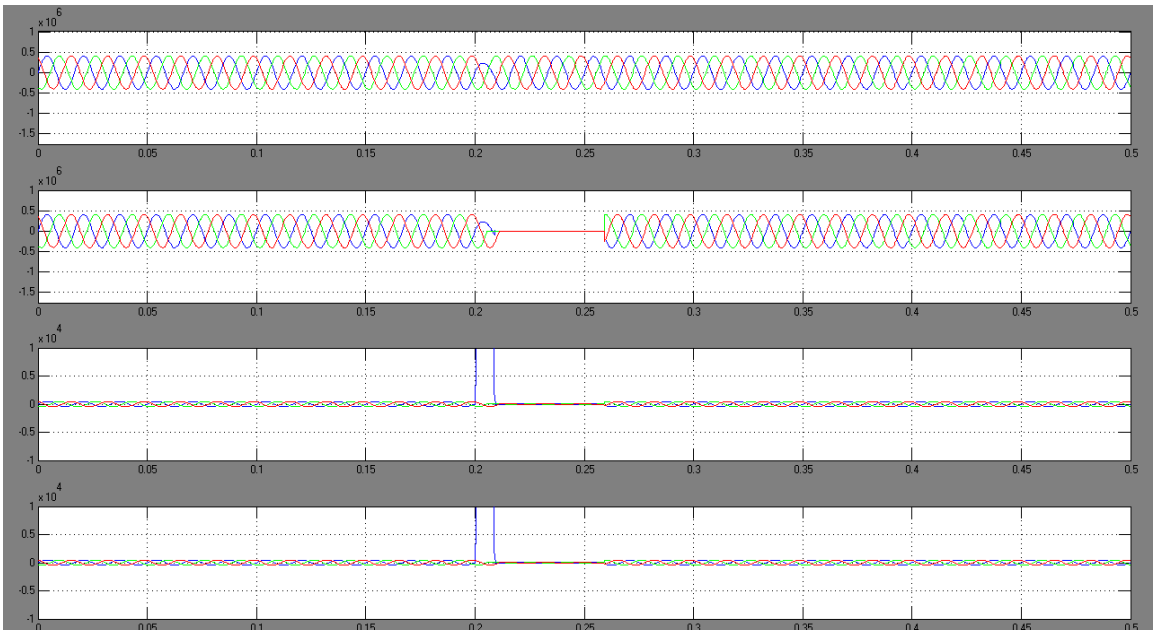


Figure 5.5 SIL test results for two-bus power system and relay model for L-G fault

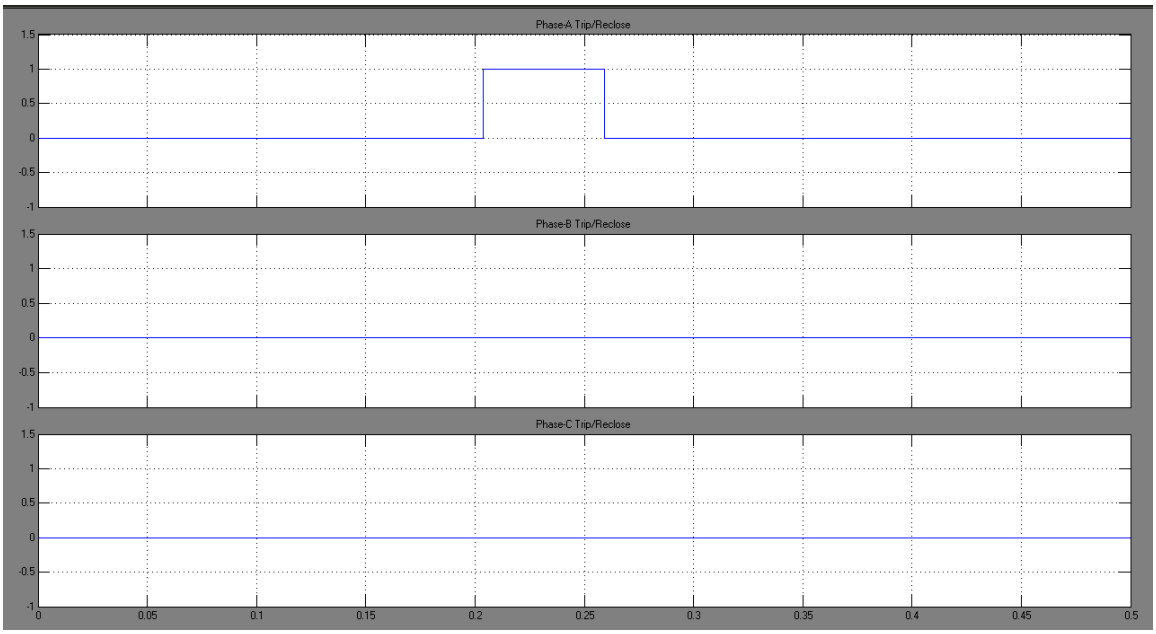


Figure 5.6 Trip/Reclose signal given by relay model for L-G fault on phase-A

The SIL test is conducted for an L-L-G fault on phases A and C for the same two-bus system. Figure 5.7 shows the generator voltages and currents, load voltages and currents for a double line to ground fault on phases A and C. The fault is injected at 0.3 secs. The relay model recognizes the fault and clears it with half-a-cycle of occurrence of the fault. The system is returned to normal operating condition at 0.35 secs. Figure 5.8 shows the trip/reclose signal issued by Matlab/Simulink relay model for L-L-G fault on phases A and C.

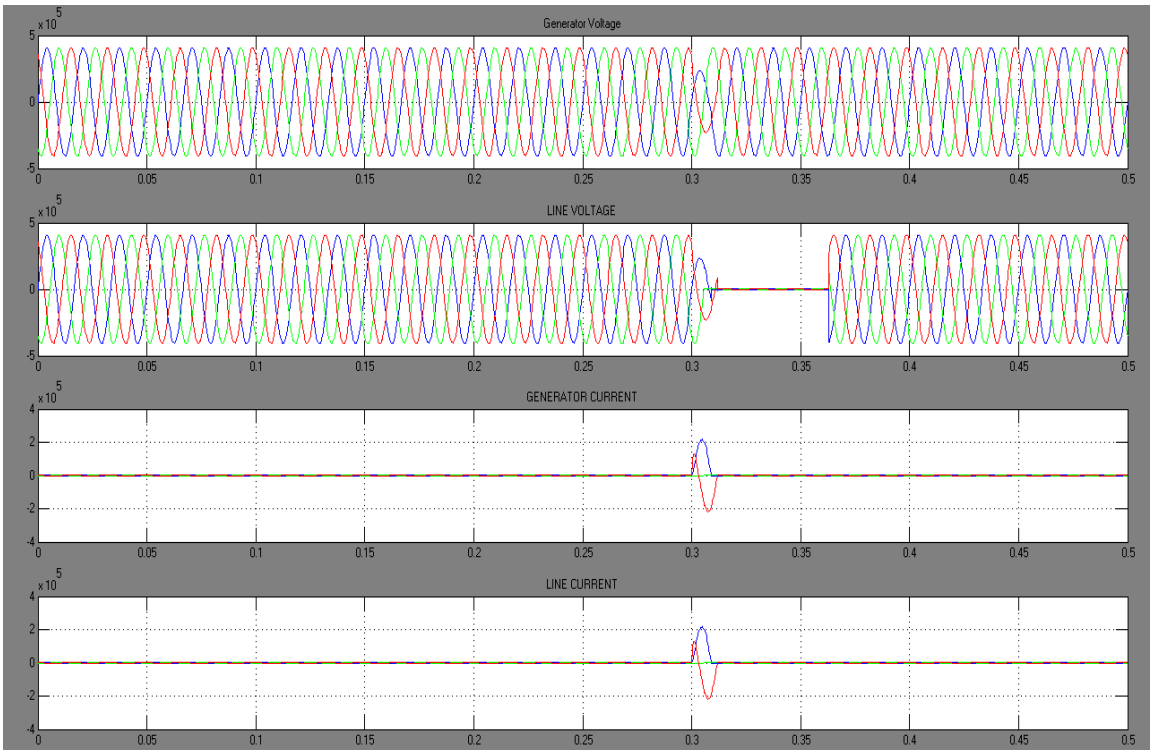


Figure 5.7 SIL test results for two-bus system and relay model for L-L-G fault

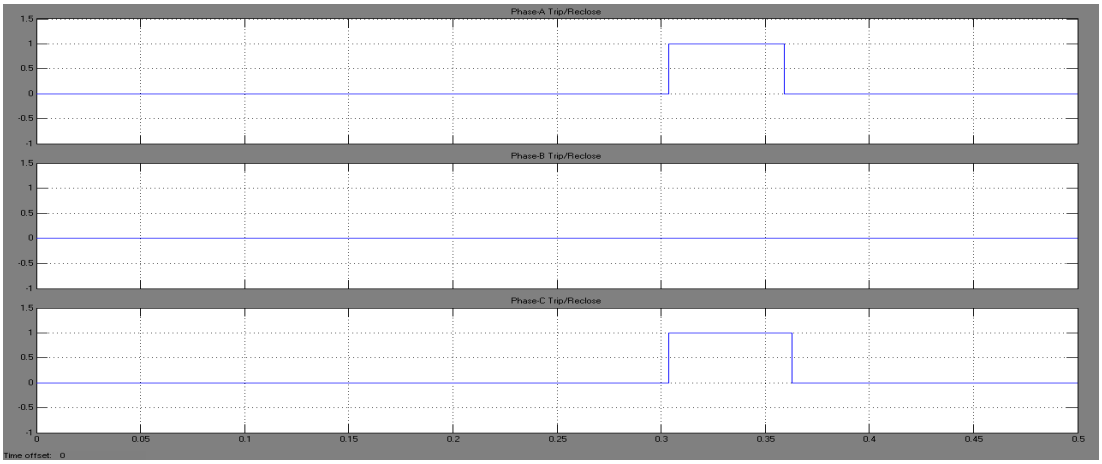


Figure 5.8 Trip/Reclose signal for L-L-G fault on phases A and C

SIL testing was also done for three-phase to ground fault on the two-bus power system but not presented here.

5.3.2 Testing with Eight-bus power system

The overcurrent relay model in Matlab/Simulink is also tested with eight-bus power system. Figure 5.9 represents the set-up for SIL testing between eight-bus system and relay model. The power system test case used in this section is the same one that is mentioned in Chapter III, Figure 3.5. The relay model output is fed into the circuit breaker-8 (as shown in Figure 5.4) by passing through a data conversion block. The fault is injected into the system at 0.7 secs of the simulation time.

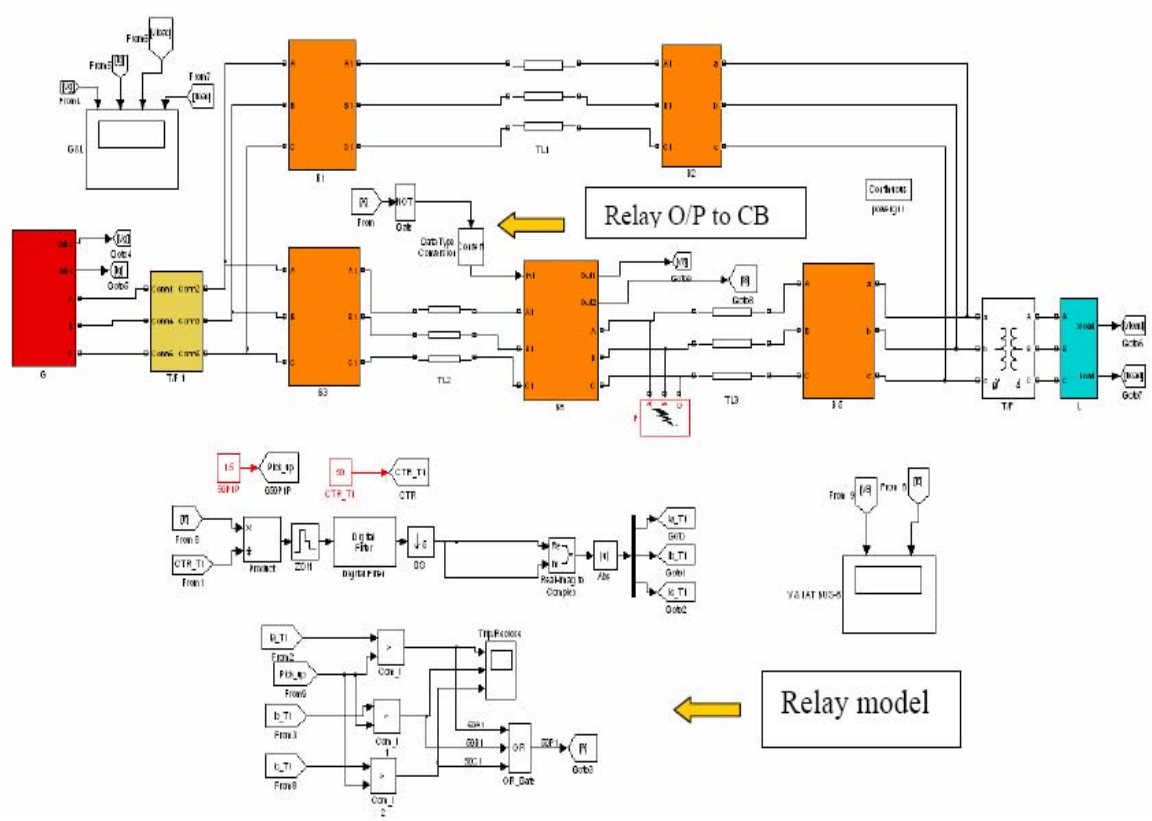


Figure 5.9 SIL test between eight-bus power system and relay model

Figure 5.10 depicts the system three-phase voltage and three phase currents upon occurrence of L-G fault on phase-A at bus-8. The C.T ratio is kept at 50:1. The pick up current is 1.5 times the nominal value. The relay model detects the fault and issues a trip signal at 0.74 secs. The system is approximately tripped at 0.747 secs. The relay again recloses the system at 0.77 secs. Figure 5.11 represents the trip/reclose signal issued by relay model on occurrence of L-G fault on phase-A.

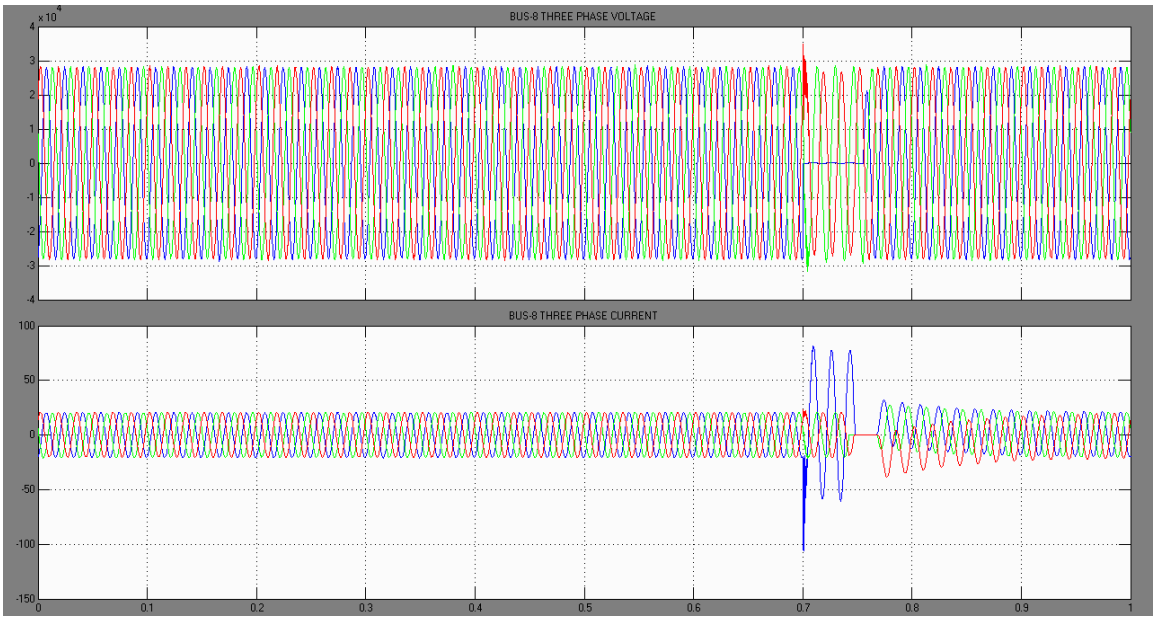


Figure 5.10 SIL test results for eight-bus power system and relay model for L-G fault

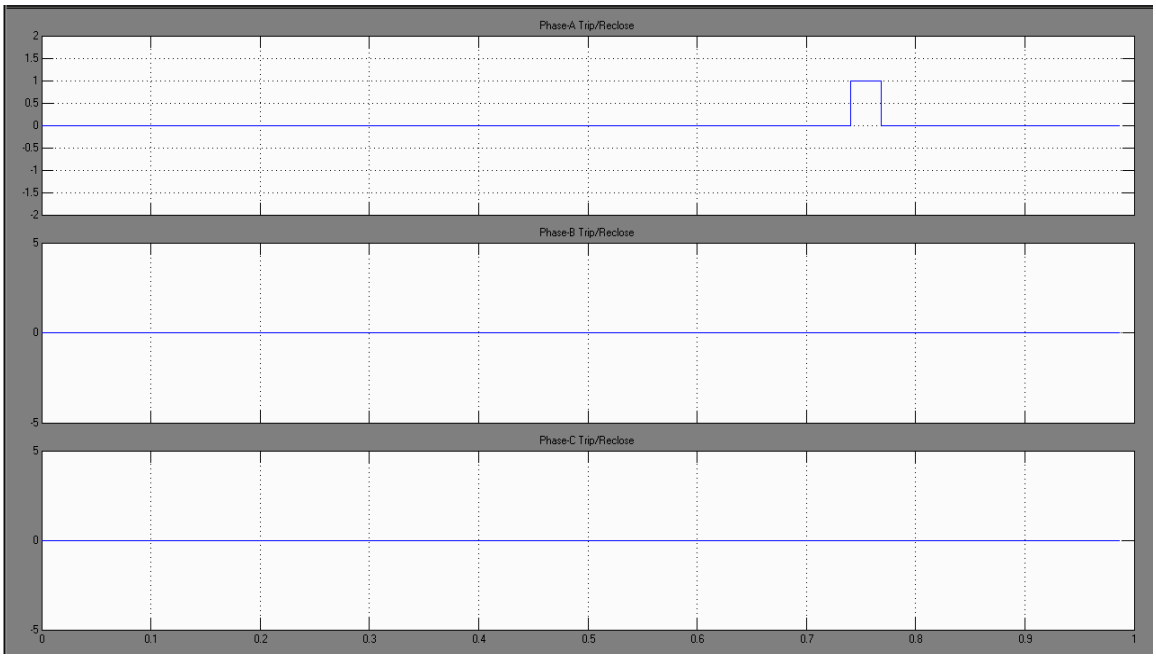


Figure 5.11 Trip/Reclose signal given by relay model for L-G fault on phase-A

SIL testing was also done for L-G, L-L-G faults on other phases on the eight-bus power system but not presented here.

5.3.3 Testing with Shipboard power system

In this section, the SIL test is conducted between the four-bus shipboard power system and relay model. The procedure followed is the same as it was followed for the previous two sections. In-depth explanation of shipboard test case is given in Chapter III. Figure 5.12 shows the set-up of SIL test between SPS and relay model in Matlab/Simulink environment.

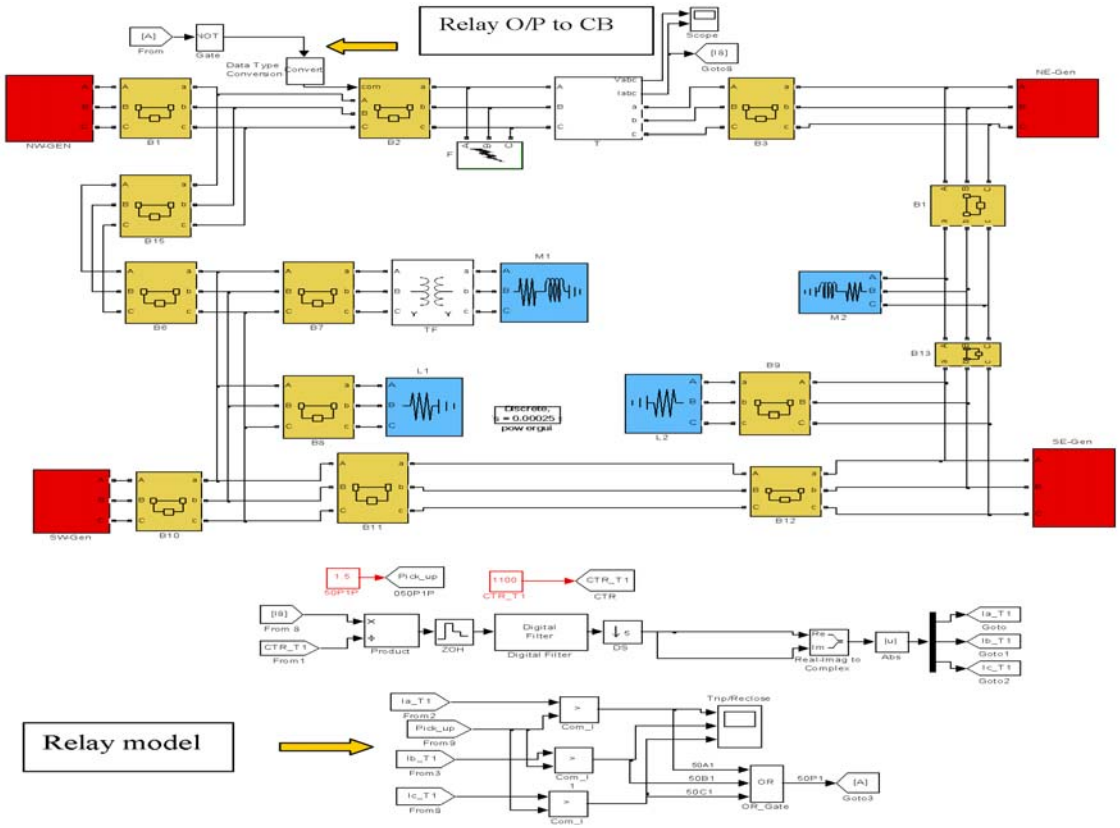


Figure 5.12 SIL test between SPS and relay model

In the relay model, the C.T ratio is set to 1100:1 and pick up current is about 1.5 times the normal value. L-L-L-G fault is injected into the system at bus-2 at 0.25secs. Figure 5.13 shows the system three-phase current at the faulted bus.

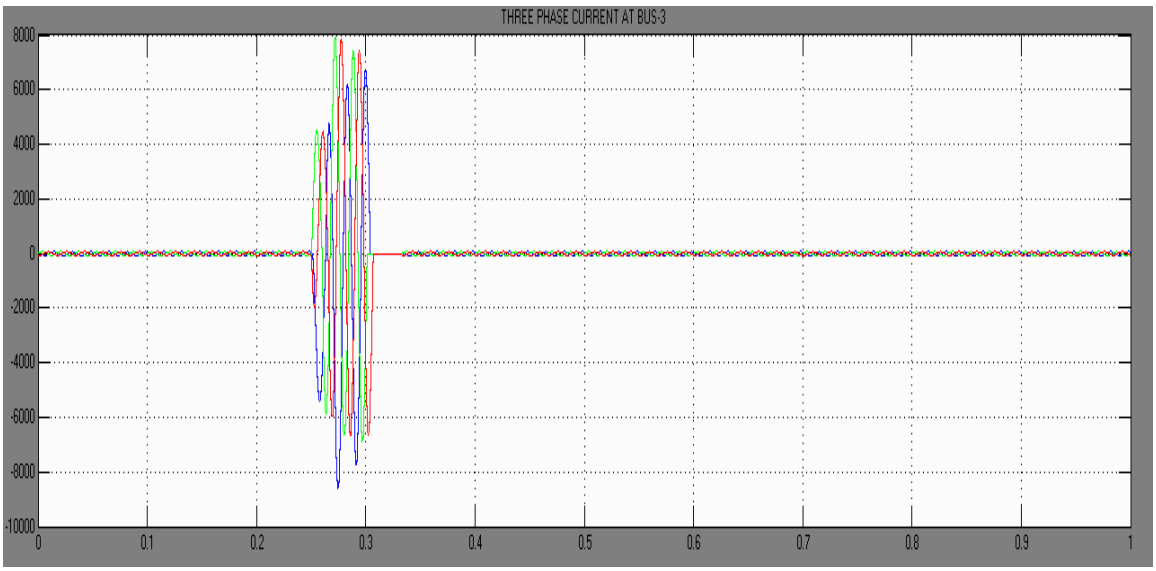


Figure 5.13 SIL test results for SPS and relay model for L-G fault

The system is tripped at 0.3 secs approximately. The system recloses again at 0.335 secs. Figure 5.14 shows the corresponding trip/reclose signal for L-L-L-G fault on phases-A, B, C on shipboard system.

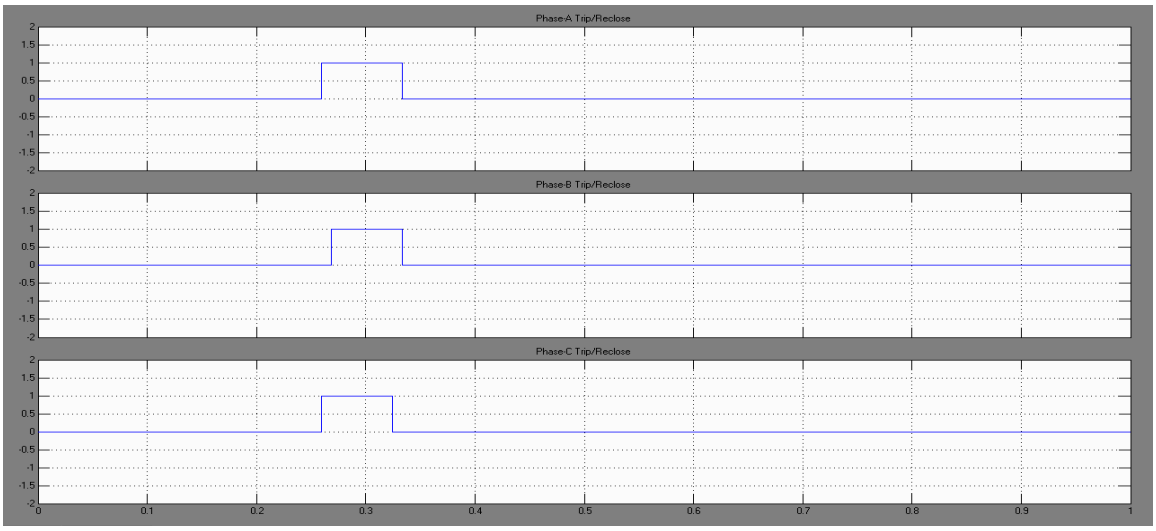


Figure 5.14 Trip/Reclose signal given by relay model for L-L-L-G fault

5.4 Summary

The simulation results of power system test cases developed in Matlab/Simulink software are presented. The LabVIEW user interface results for all the power system test cases are presented. These LabVIEW front panels are very useful while running the power system models in real-time for conducting a variety of HIL tests. The performance of the instantaneous overcurrent relay model is tested by conducting a closed loop simulation with different power system models in Matlab/Simulink environment. The relay model is performing well for smaller power systems with basic relay functionality. In case of larger power systems, the relay model performance is not as expected. It takes 3 to 4 cycles to trip the eight-bus system when compared to ½ a cycle for two-bus power system. There is a need to develop much more reliable relay model for better performance.

CHAPTER VI

SIMULATION RESULTS FOR NI-PXI AS RELAY MODEL

6.1 Introduction

The previous chapter presents the no-fault simulation results and SIL test results for different power systems with overcurrent relay model developed in Matlab/Simulink This chapter deals with simulation of the LabVIEW relay model that is introduced in chapter IV. The first section of this Chapter presents the results of the LabVIEW relay model in internal mode of operation. The next sections show the results of closed loop testing done between RTDS and the LabVIEW relay model (external mode of operation) and finally relay model validation.

6.2 Performance of LabVIEW Relay Model in Internal Mode of Operation

In this section, the simulation results of the LabVIEW relay model in internal mode of operation are presented. In-depth discussion about internal mode is given in section 4.5 of Chapter IV.

6.2.1 L-G fault

In the internal mode of operation, the current signals fed to the relay model come from internal signal sources. Through the option provided on the relay model, an L-G

fault is placed on phase-A. Figure 6.1 shows a phase-A fault on the system and corresponding trip signal. The fault is injected into the system at 0.1 sec of the simulation time. It is evident from the figure that the fault is immediately detected and corresponding trip signal is generated.

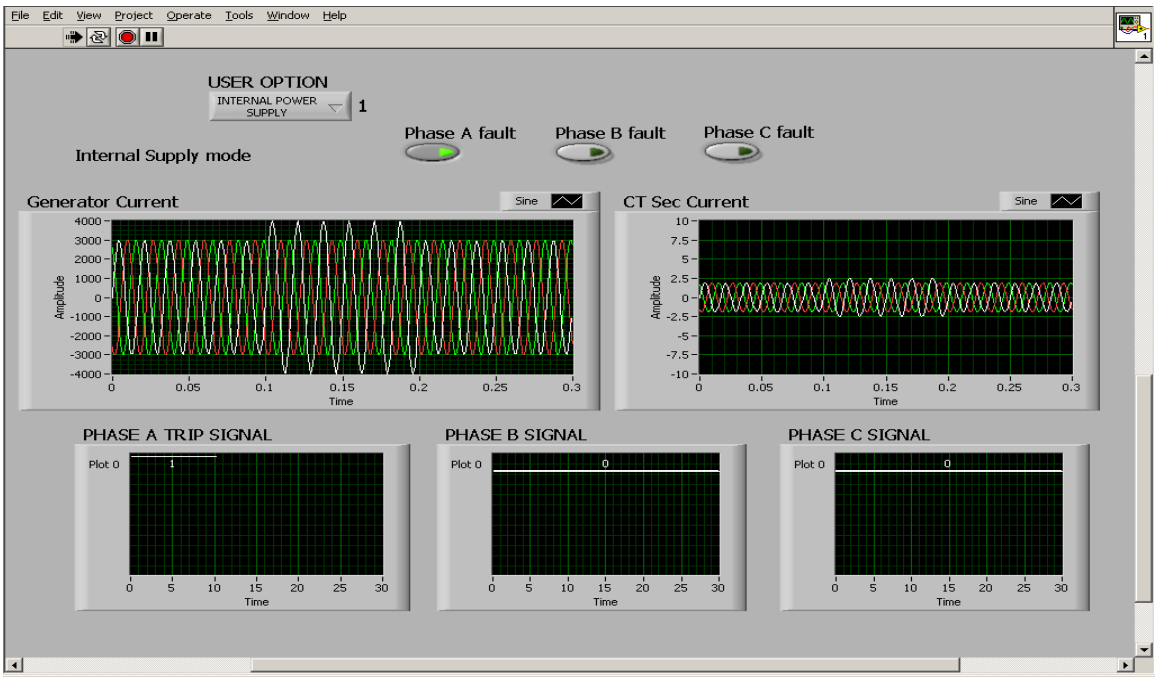


Figure 6.1 Internal mode of relay model showing phase-A fault

6.2.2 L-L-G fault

LabVIEW relay model testing in internal mode of operation is also done with a double line to ground fault. In this case an L-L-G fault is placed on phases B and C. The fault is injected at the same time as the previous case (i.e.) 0.1 sec of the simulation time. Figure 6.2 shows the screenshot of the LabVIEW relay model in internal mode of

operation for L-L-G fault. The fault is visible in generator current as well as in CT secondary current also.

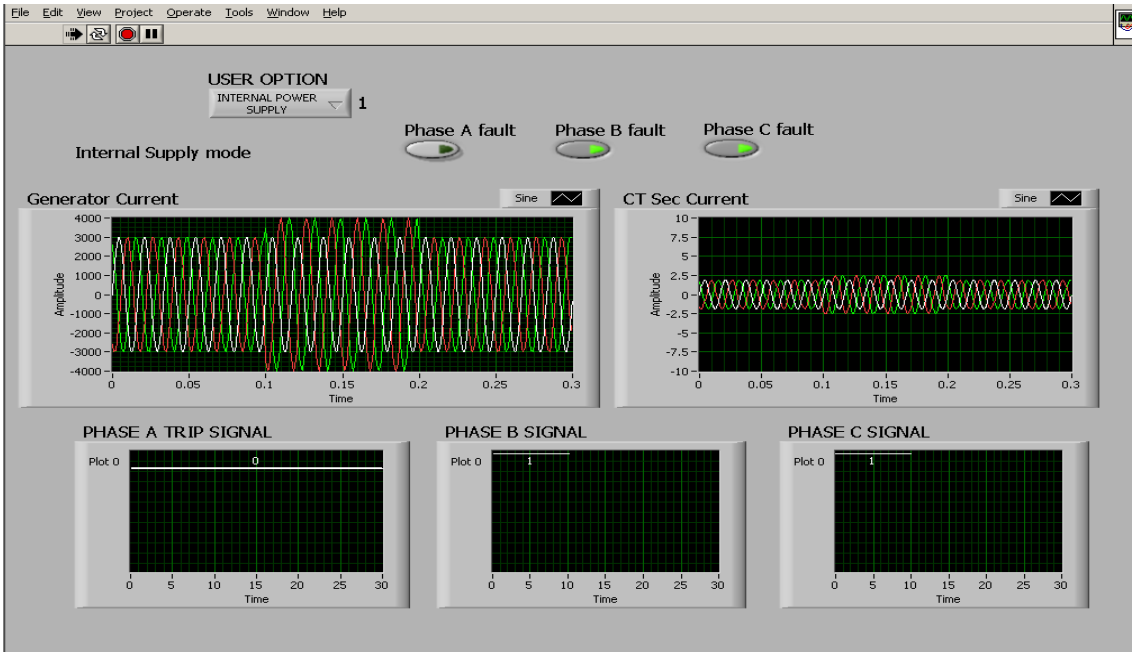


Figure 6.2 Internal mode of relay model showing L-L-G fault

6.3 Performance of LabVIEW Relay Model in External Mode

The real-time performance of the LabVIEW overcurrent relay model in its external mode of operation is discussed in this section. In this mode of operation the current signals are fed from a real-time simulator, RTDS. HIL tests are conducted to evaluate the model performance. These HIL tests also help in validating the developed model. The procedure followed to validate the relay model consists of two tests, National Instruments Controller-in-the-Loop (NICIL) test and SEL Relay-in-the-Loop (SELRIL)

test. In the basic HIL test, if the hardware is a National Instrument controller then it is a NICIL test and if the hardware is an SEL relay then it is an SELRIL test.

6.3.1 NICIL Test Results

The relay model is subjected to NICIL testing with an eight-bus power system running in real time on the RTDS (section 3.5, chapter III) and LabVIEW overcurrent relay model running in real time on NI-PXI Controller. In this National Instruments Controller-in-the-Loop test, a real time simulation environment is created by protecting the power system with the relay model. Figure 6.3 shows the setup for NICIL testing. The eight-bus power system model (Figure 3.8) is run on the RTDS in real time. The developed overcurrent relay model is downloaded to an NI-PXI-8196 controller. The current signals taken from the RTDS are fed into the relay model running on the NI-PXI-8196 controller.

Figure 6.3 Setup for NICIL testing

The NI PXI-1042Q is an 8-slot chassis. The NI PXI-8196 controller is installed in the system controller slot of NI PXI-1042Q chassis. The NI PXI-6251 is an M-series multifunctional data acquisition device. The NI PXI-6608 is a high precision counter/timer with digital I/O. The current signals coming from RTDS are routed to NI PXI-6251 DAQ device through the SCB-68 (Shielded I/O connector block for DAQ devices with 68-pin connectors) interconnector. The relay model samples the current signal and provides appropriate trip and reclose signals. The trip and reclose signals are generated using NI PXI-6608. These digital signals generated by the relay model are fed into RTDS digital channels.

A NICIL test is conducted for a single phase to ground fault on phase C. Figure 6.4 shows single-phase currents at bus-8 for a single-phase to ground fault on phase C. The fault location is at 50% of the transmission line with a fault resistance path of 0.1Ω. The fault occurs at 0.2 sec. The relay immediately recognizes the fault and trips the system at 0.33 secs. This is an instantaneous operation as the fault detection/action period is about 0.1sec, 6 cycles on a 60Hz base. The system recloses at 0.438 sec. The transient override is set as 1 in this test. It allows the relay to give a trip if the fault is for more than one cycle. If the fault is only for 1 cycle then the relay thinks it is a transient and does not give a trip signal. Eventually the transient dies and the system is restored to its normal operation. These trip and reclose signals are falling edge signals. Figures 6.5 represents the digital trip and reclose signals given by relay model and as seen on RTDS -RUN window.

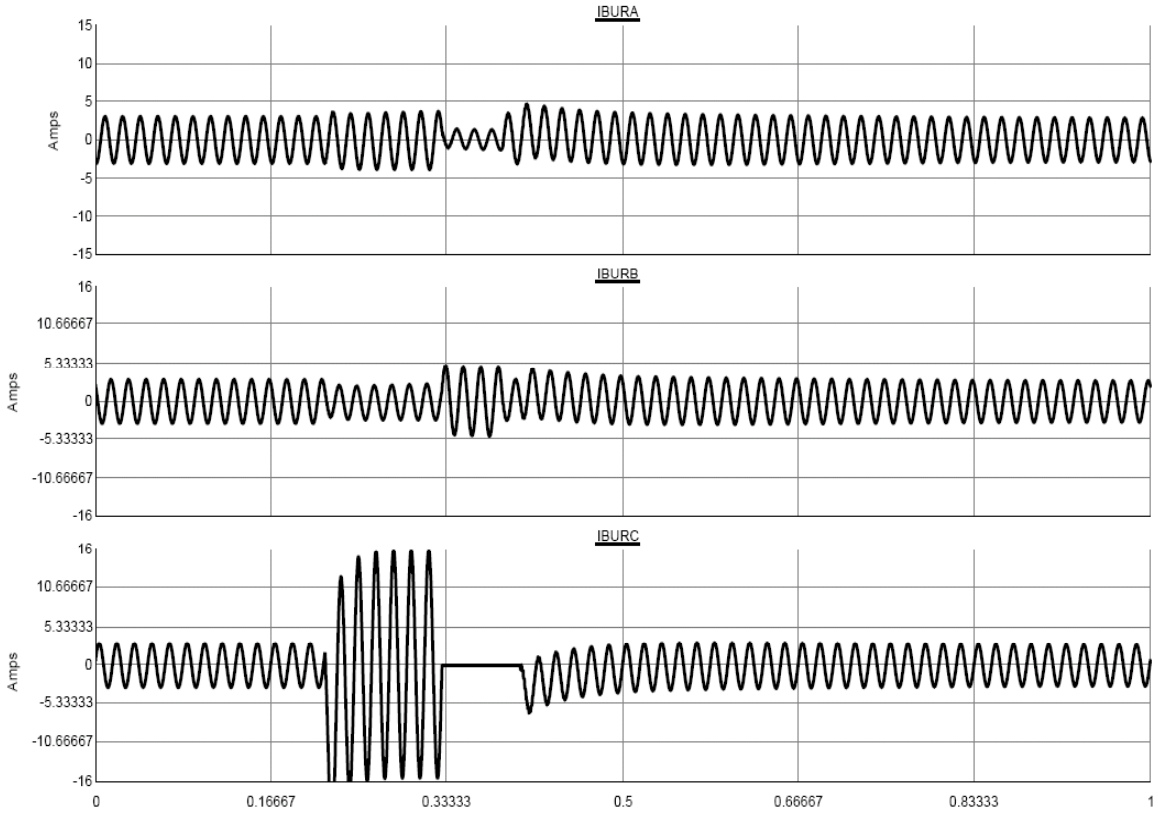


Figure 6.4 Single-phase currents at bus-8 for a L-G fault on 'phase- C'.

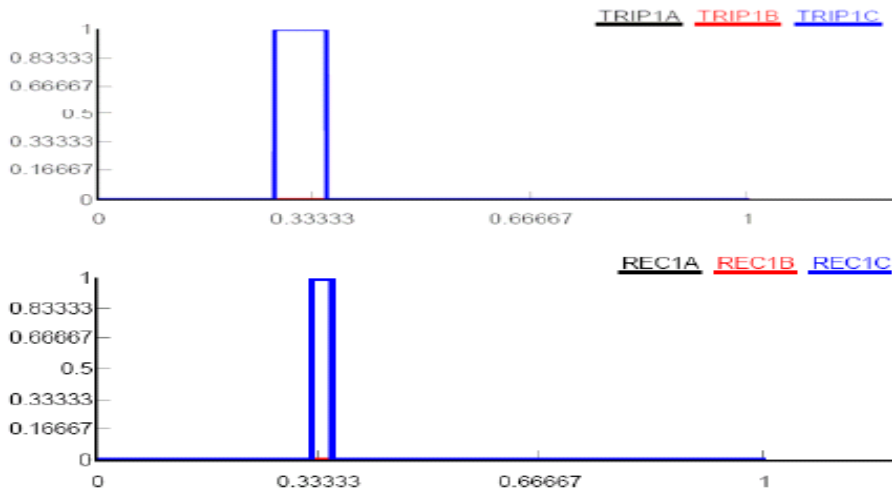


Figure 6.5 Trip and reclose signals given by relay model.

As the fault occurs on the system, the system becomes unbalanced. This is the reason for the disturbances of phase A and phase B currents in figure 6.4 due to a single phase to ground fault on phase C. The relay model has excellent fault detection mechanism and the NICIL test results demonstrate its capacity.

6.3.2 SELRIL Test Results

To validate the instantaneous/time delay overcurrent relay model, the SELRIL test is conducted between the RTDS (power system) and SEL 351S relay. These SELRIL test results will help develop the best possible model for the overcurrent relay. The setup for the SELRIL test is shown in Figure 6.6

Figure 6.6 Setup for SELRIL test

Figure 6.7 shows the results of SELRIL test with a single phase to ground fault on phase C. The power system used in this SELRIL test is the same as the power system used in NICIL testing. The single phase to ground fault occurs at 0.4 sec of the simulation

time. The trip signal is issued at 0.47 sec. The reclose signal comes at 1.62 sec (i.e.) after a time gap of 1.147 sec (69 cycles on a 60Hz base), the system again recloses and returns to its normal state of operation.

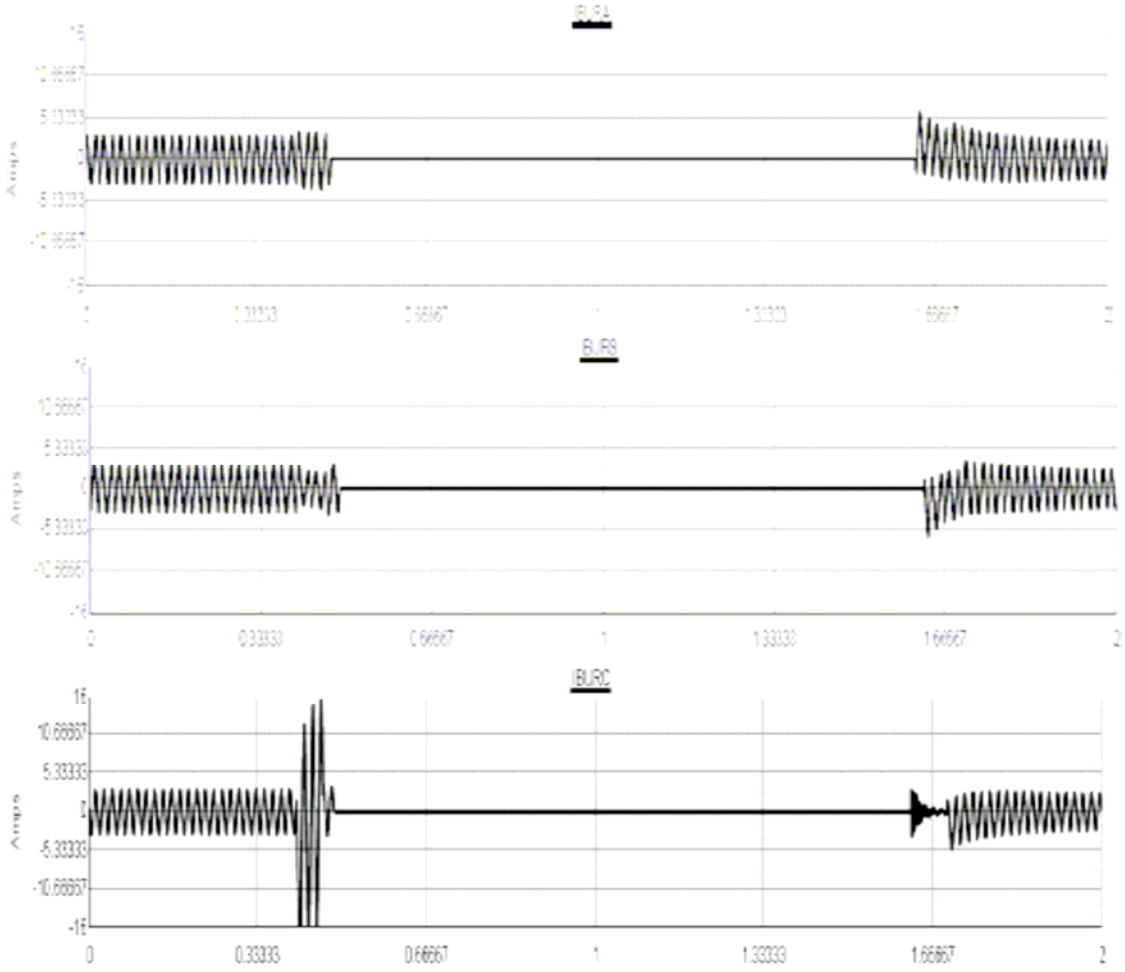


Figure 6.7 Single-phase currents at bus-8 for L-G fault on phase C.

Figure 6.8 shows the corresponding trip and reclose signals given by SEL- 351S overcurrent relay for a single phase to ground fault on phase C.

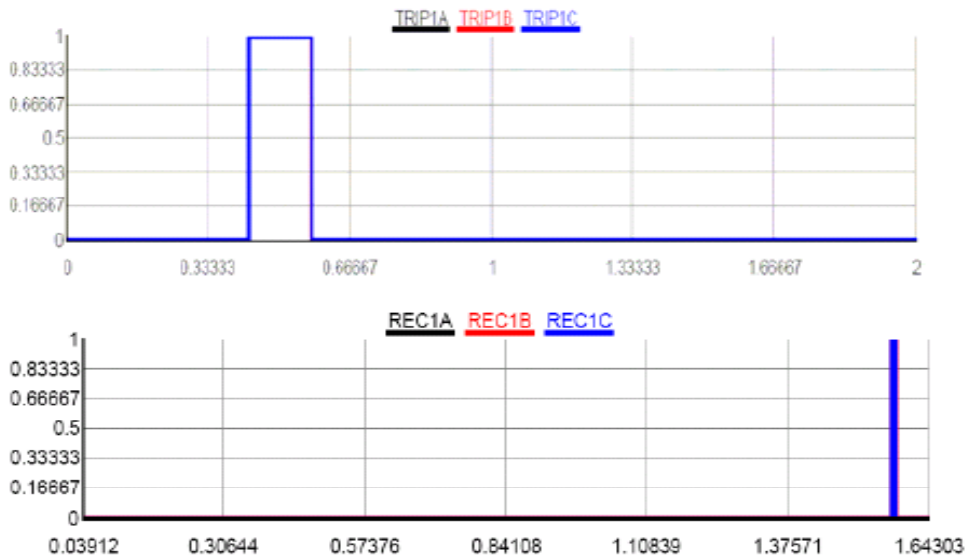


Figure 6.8 Trip and reclose signals for SELRIL test

6.3.3 Relay Model Functionality Validation

Comparing the results of both the SELRIL and NICIL tests can provide model validation. The performance of the relay is a good first order model for the SEL-351S relay. The fault detection periods of the relay model and the SEL 351S are almost the same. Depending on the application, some systems need faster reclose and some need slower reclose. The relay model can be designed for faster reclosing or slower reclosing. In the NICIL test, the model was designed for faster reclose. The reclosing time for overcurrent relay model is 0.1 sec after the system is opened while it is 1.1 sec for the SEL-351S relay. The LabVIEW instantaneous/time delay overcurrent relay is very flexible and can be designed according to the requirements of the user.

6.4 Summary

In this chapter, simulation results of different modes of operation of the LabVIEW relay model are presented. The internal mode of testing is done for L-G and L-L-G faults. In order to validate the relay model functionality in external mode, NICIL and SELRIL tests are conducted. The results have demonstrated that the overcurrent relay model can provide a first order approximation for a commercial overcurrent relay. The developed model can be useful for HIL testing, where cost and time implications come into effect.

CHAPTER VII

SIMULATION RESULTS FOR NI-PXI AS POWER SYSTEM SIMULATOR

7.1 Introduction

This chapter details the setup procedure for building an HIL platform using NI-PXI in real-time. The necessary and sufficient results to establish NI-PXI as a power system simulator are shown in this chapter. The closed loop test results conducted between NI-PXI and dSPACE, with the relay model running on dSPACE and power system model running on NI-PXI are also presented. To strengthen the developed HIL platform for power system simulations, HIL tests are conducted between NI-PXI and SEL-351S relay. The HIL test setup and the results of the two-bus power system for different fault conditions are presented.

7.2 NI-PXI Real-Time Platform Setup

7.2.1 Procedure for Platform Set-up

On the developed NI-PXI real-time platform, Simulink models can be run in real-time and can be further used for HIL testing purposes. To run a Simulink model on a RT

target, there is a need to convert that Simulink model into a Dynamic Link library (DLL) that LabVIEW can call. Figure 7.1 shows the block diagram of HIL setup using NI-PXI controller. To create a model DLL, real-time workshop converts the Simulink model and any of its sub-models into C code. Then Microsoft Visual C++ compiles the C code into a model DLL named A.dll, where A is the name of the Simulink model.

Converting a Simulink model into A.dll will result in creating a simulation model, which can run on an RT target. SIT server creates M.VI (Model Virtual Instrument) and D.VI (Driver Virtual Instrument), which are used to communicate with A.dll. Using the host VI, the M.VI and the A.dll are downloaded to an RT target. The M.VI starts the Simulation Interface Toolkit (SIT) server on an RT target, calls a D.VI that calls the A.dll, and then stops the SIT server when the simulation stops. The D.VI interacts with the A.dll and exchange parameter information between the host VI and the A.dll on the RT target [2], [30]. Thus Simulink models are run in real-time and these models can interact with any physical devices such as relays.

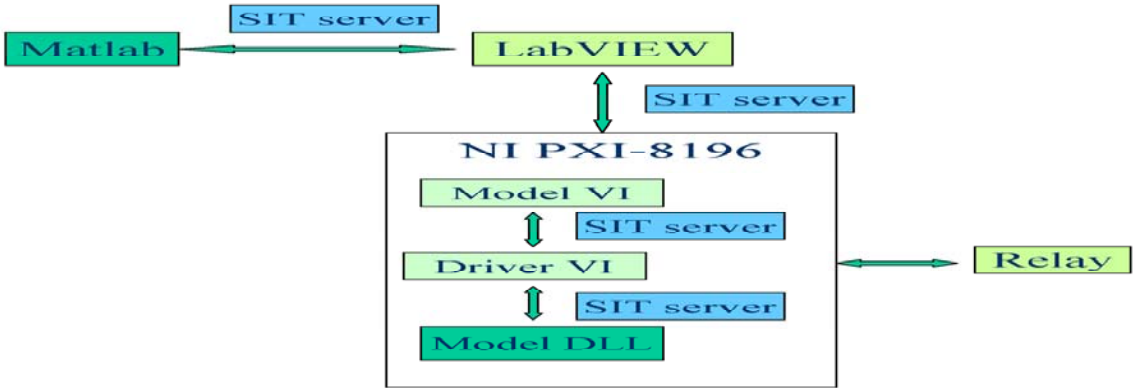


Figure 7.1 Block diagram of HIL setup using NI-PXI controller [2], [30].

7.2.2 Trouble Shooting for Errors during Platform Set-up

While dealing with LabVIEW, SIT and real-time targets, the users might come across different errors. The troubleshooting procedures for some errors are explained in detail.

- SIT server not starting in Matlab command window.

Solution: The SIT software should be installed using the guidelines mentioned in help file. If the SIT server did not start in Matlab command window then type the following command

NISITServer('start', xxxx)

Where "xxxx" represents the required port number. The default port for SIT is 6011. To intentionally stop the SIT server, type the following command

NISITServer('stop')

- LabVIEW VI screen graying out

Solution: Open the Simulink model and browse through configuration parameters. In the 'Optimization' tab, uncheck "Block Reduction" and "Signal storage reuse".

- Error 63

Solution: In the SIT connection manager, browse to simulation environment and check for port number. Default port number is 6011. SIT should also run on the same port. Browse through 'Tools-options-VI server configuration-Protocols'. Check the TCP/IP option. Also make sure that port number is 6011. Check all the options in it. Give access to all users by placing * in the VI Server: Machine access and VI Server: User access.

- Error 56

Solution: This error occurs while communicating between host VI and NI-PXI 8196 target using TCP/IP protocol. This is an issue between Time-Critical loop and the Normal priority loop VIs. The best way to solve this error is to transfer less data so that TCP/IP operations can be completed within the required time.

7.3 NI-PXI as a Power System Simulator

For power system simulation, different types of real-time simulators are used like Open Scalable Real Time Simulator (Opal RT), RTDS etc [39]. Another real-time simulator is NI-PXI, where Matlab/Simulink models can be deployed using SIT. In this section of the chapter, NI-PXI is established as a real-time power system simulator by simulating similar power systems on RTDS and NI-PXI for double line to ground (L-L-G) fault and for the three-phase to ground (L-L-L-G) faults. The results obtained by both the simulations are analyzed and the performances of real time simulators are evaluated [40].

7.3.1 Modeling Procedures and Test Cases

RTDS and NI-PXI follow different approaches for modeling. The software used to model power system in RTDS is RSCAD, which has in-built library for power system components. To run a power system on NI-PXI, modeling has to be done in Matlab/Simulink and the model has to be exported to NI-PXI with the user interface in LabVIEW. A detailed explanation of RTDS and NI-PXI and their real-time capabilities are mentioned in chapter II of this thesis. The RSCAD test case used in this section of the

chapter is the one mentioned in chapter III, Figure 3.8. The Matlab/Simulink test case used for NI-PXI in this section of the Chapter is almost the same as the test case mentioned in chapter III, Figure 3.4. The Matlab/Simulink test case used in this section of the chapter has step-up transformer of 13.8kV/230kV and step-down transformer of 230kV/15kV. The step-down transformer provides 1200MVA load at 15kV. The real power component of the load is 1107MW and reactive power component is 471MVAR [40].

7.3.2 Performance comparison of RTDS and NI-PXI

The eight-bus power system model developed in Matlab/Simulink and RSCAD is subjected to different faults. Running these models in real-time on the RTDS and NI-PXI, respectively can compare the simulation capability of NI-PXI with RTDS. Further these fault events occurring on these real-time simulators are recorded by connecting a SEL-351S commercial relay to the simulators [40].

7.3.2.1 L-L-L-G fault

The power system shown in Figure 3.8 is simulated by placing a three phase to ground fault at bus-8 of the system. The fault duration is from 1.0 to 1.3 secs. Figure 7.2 represents the run time window of RTDS showing a triple line to ground fault on phases A, B and C.

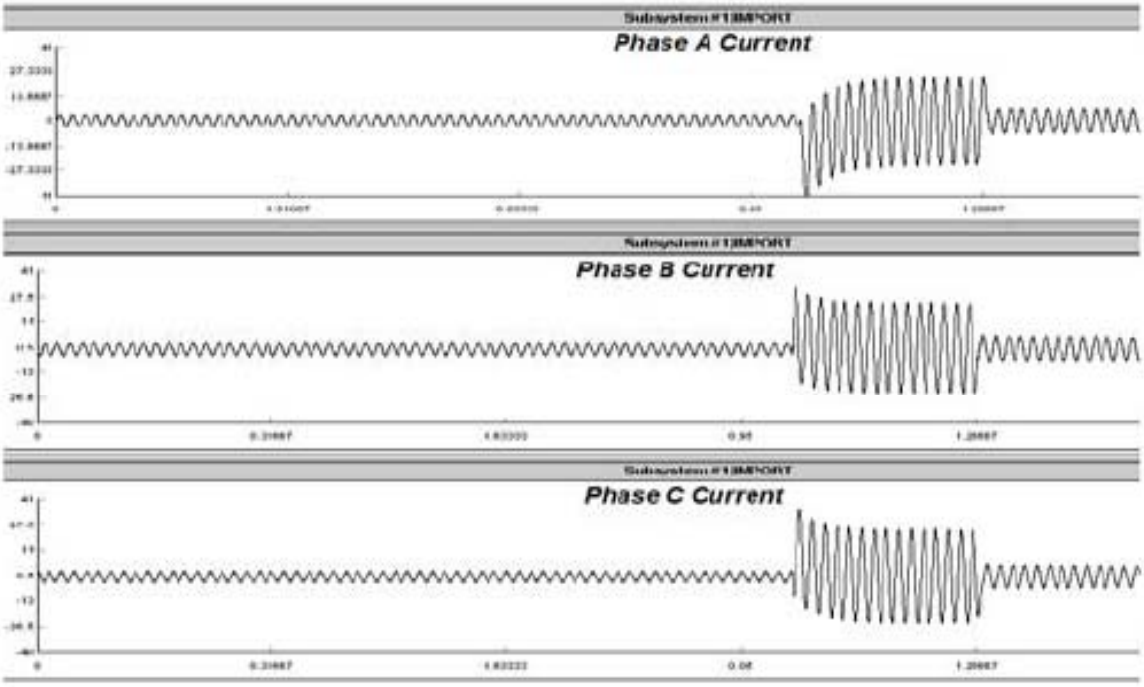


Figure 7.2 RTDS run-time window showing L-L-L-G on phases A, B and C

The three-phase current and voltage signals coming from the RTDS are connected to SEL-351 overcurrent relay. Figure 7.3 represents the corresponding SEL-351S relay report for the L-L-L-G fault on phases A, B and C. According to SEL-351S report, upon occurrence of three-phase fault on the system, the phase-A, phase B and phase C currents increase drastically and are well above the threshold value of 960A. Table 7.1 explains the digital signal codes present in SEL-351S report [41].

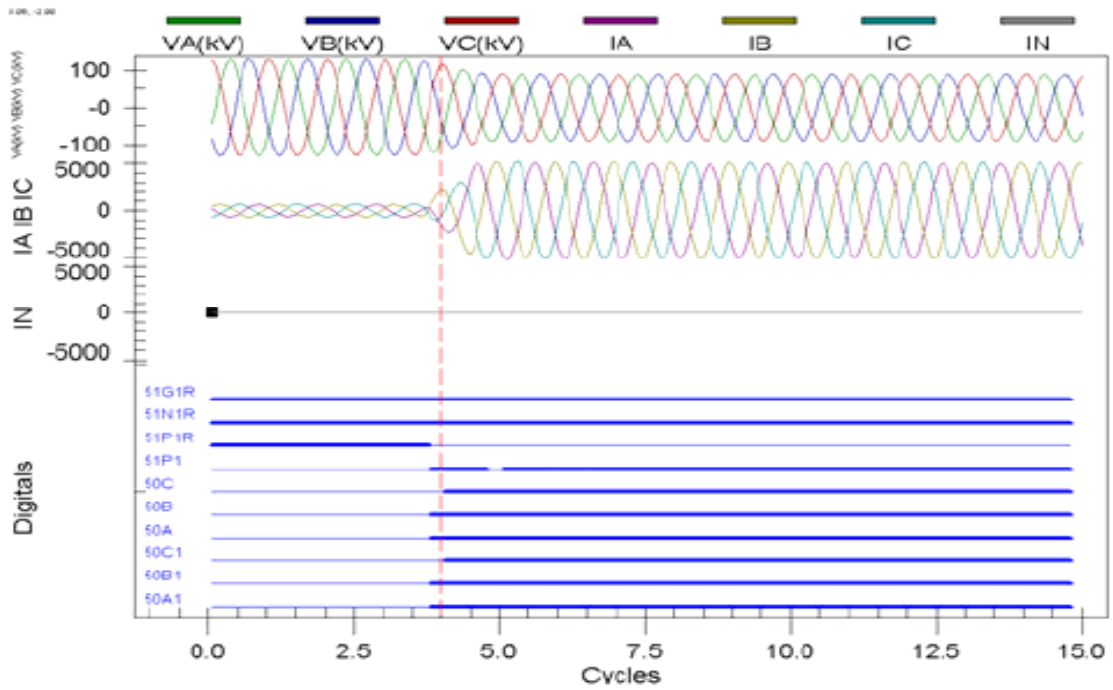


Figure 7.3 SEL-351S relay report for the L-L-L-G fault on RSCAD model.

Table 7.1 Overcurrent relay elements settings along with their definitions [41]

Setting	Definition
$\mathbf{V}_A$, V_B,$\mathbf{V}_C$	Phase Voltages
$\mathbf{I}_A$,$\mathbf{I}_B$,$\mathbf{I}_C$	Phase Currents
51GR	Residual ground time over-current element
51G1R	Residual ground time over-current element 51G1T reset
51P1	Maximum phase current above pickup setting 51P1P for phase time over-current element 51P1T
51P1R	Phase time over-current element 51P1T reset
51NIR	Neutral time over-current element 51N1T reset
50A	Sum of the A-phase instantaneous over-current element for Level 1, 2, 3 and 4
50A1	Level-1 A-phase instantaneous over-current element
51N1T	Neutral time over-current element 51N1T timed out
51P1T	Phase time over-current element 51P1T timed out

By considering the definition of digital signals (51P1, 50A, 50B, 50A1, 50B1) in Table 7.1, and applying it to Figure 7.3, it is obviously evident that a triple line to ground fault occurred on the system on phases A, B and C [40].

To determine the simulation capability of the NI-PXI, the Matlab/Simulink power system model is subjected to a triple line to ground fault and the model is made to run in real-time on the NI-PXI. Figure 7.4 shows the corresponding real time simulation response on NI-PXI for L-L-L-G fault on phases A, B and C [40].

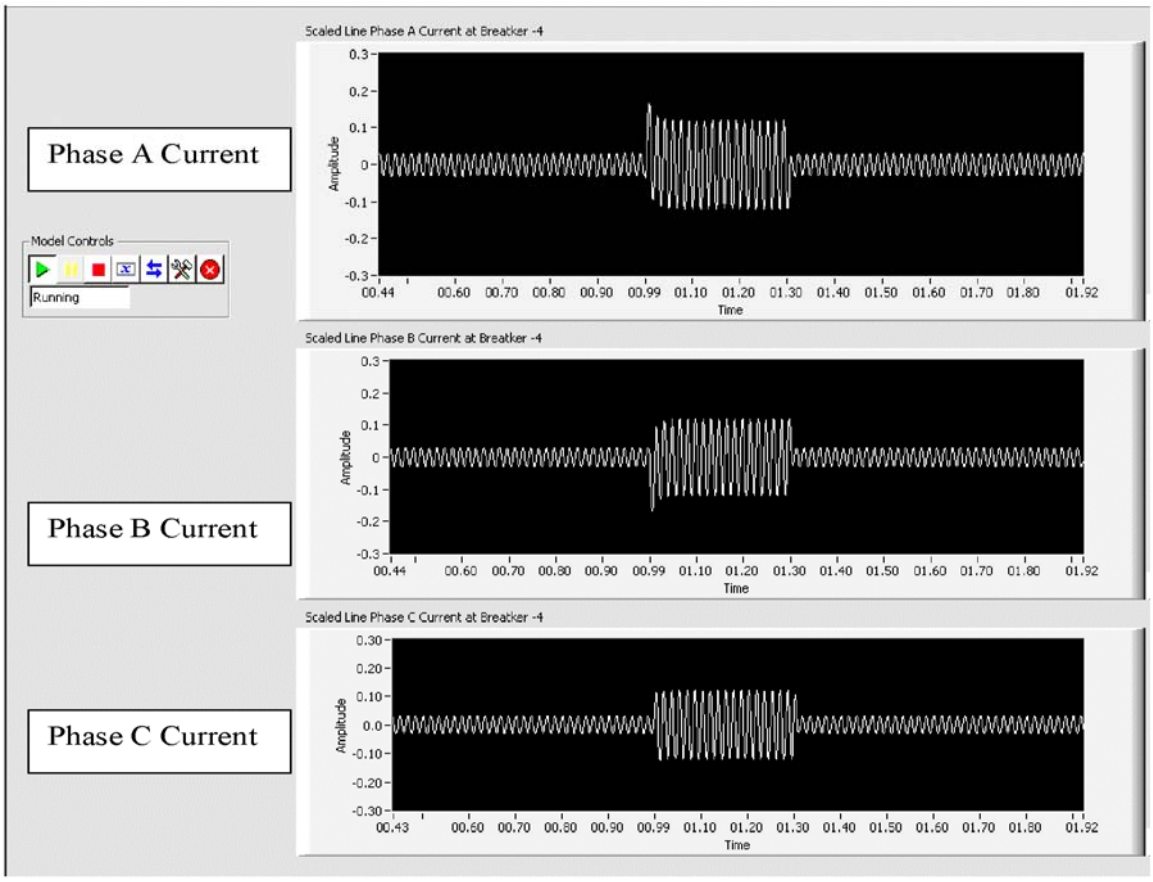


Figure 7.4 LabVIEW user interface showing L-L-L-G on phases A, B and C

The fault duration is same (i.e.) from 1.0 to 1.3 secs. The fault resistance is 0.001Ω. The fault report recorded in SEL-351S for the L-L-L-G fault on NI-PXI is shown in Figure 7.5. During the fault, all the phase currents increase and are well above the threshold value.

It is also evident in the voltage waveforms that the phase A, phase B and phase C voltages go down abruptly during the fault [40].

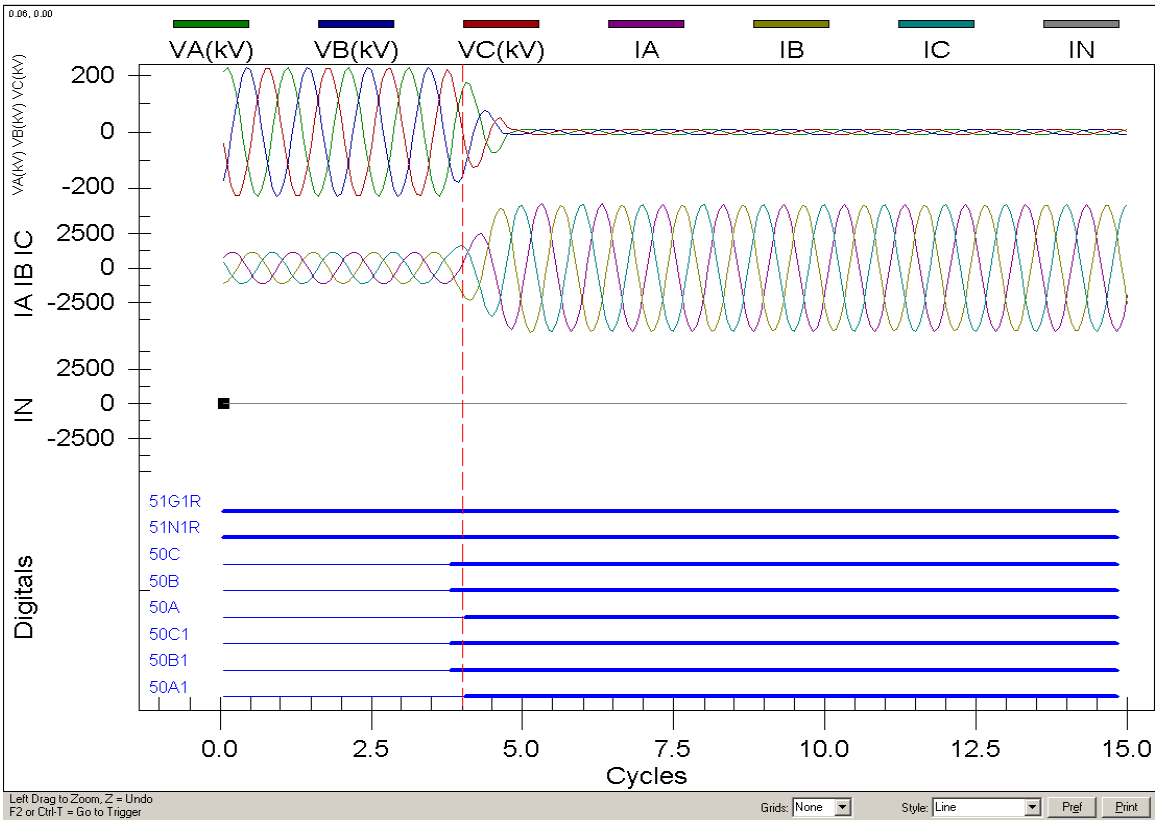


Figure 7.5 SEL-351S report for L-L-L-G fault in Matlab/Simulink model

The eight-bus system is simulated on the NI-PXI and SEL-351S could record the fault events as it did with RTDS. It is recommended that the scaling factor should be

appropriate so that the simulated currents lie within the DAQ card ranges [40]. Also note that the differences between the NI-PXI and the RTDS results are expected due to the modeling limitations of Matlab/Simulink. The transient simulation capability of Matlab/Simulink is not as accurate and precise as that of the RSCAD. This leads to slight differences in the electrical circuit behavior during fault analysis.

7.3.2.2 L-L-G fault

In this section, the power system test case in RSCAD is subjected to a double line to ground fault. Figure 7.6 shows a double phase to ground fault in RSCAD model.

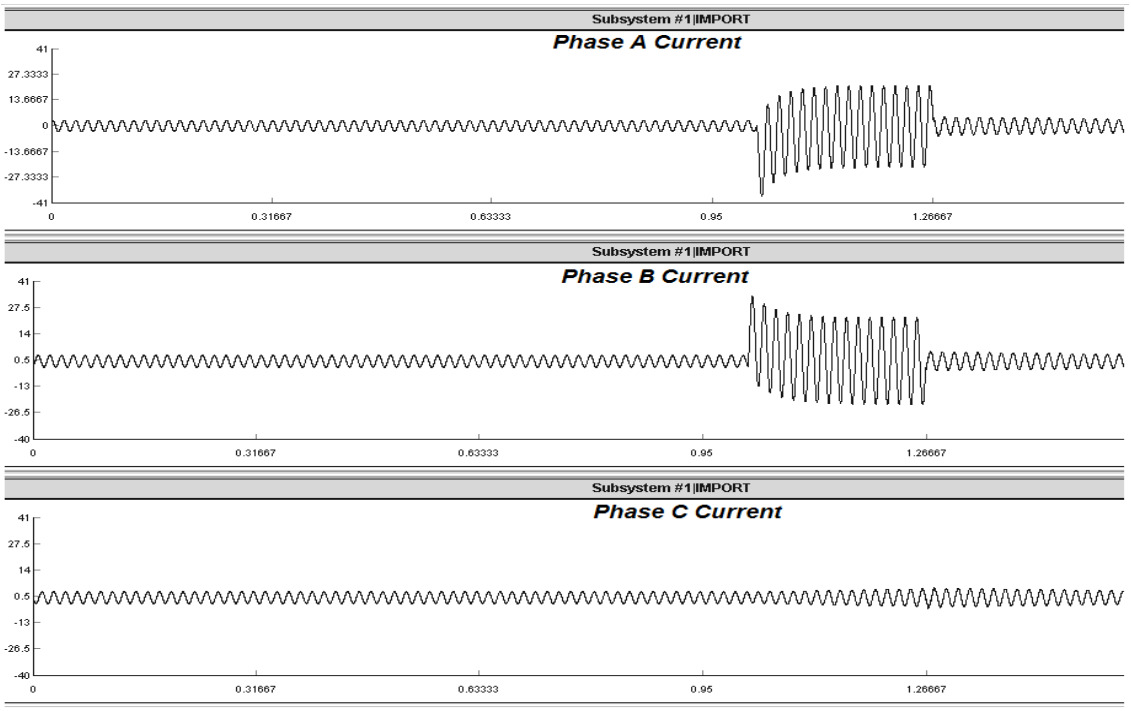


Figure 7.6 RTDS run-time window showing L-L-G on phases A and B

The report taken from SEL 351S for the simulated double line to ground fault on RTDS shows that the phase A and B currents increase above the pickup value of the relay. The phase C current remains normal at 611A [40].

The eight-bus system test case in Matlab/Simulink is subjected to double line to ground fault with the phases A and B grounded through a fault resistance of 0.001 Ω. The fault duration is kept the same as the fault duration in triple line to ground fault simulation. Figure 7.7 depicts double line to ground fault in the LabVIEW user interface with the test case running in real time on the NI PXI.

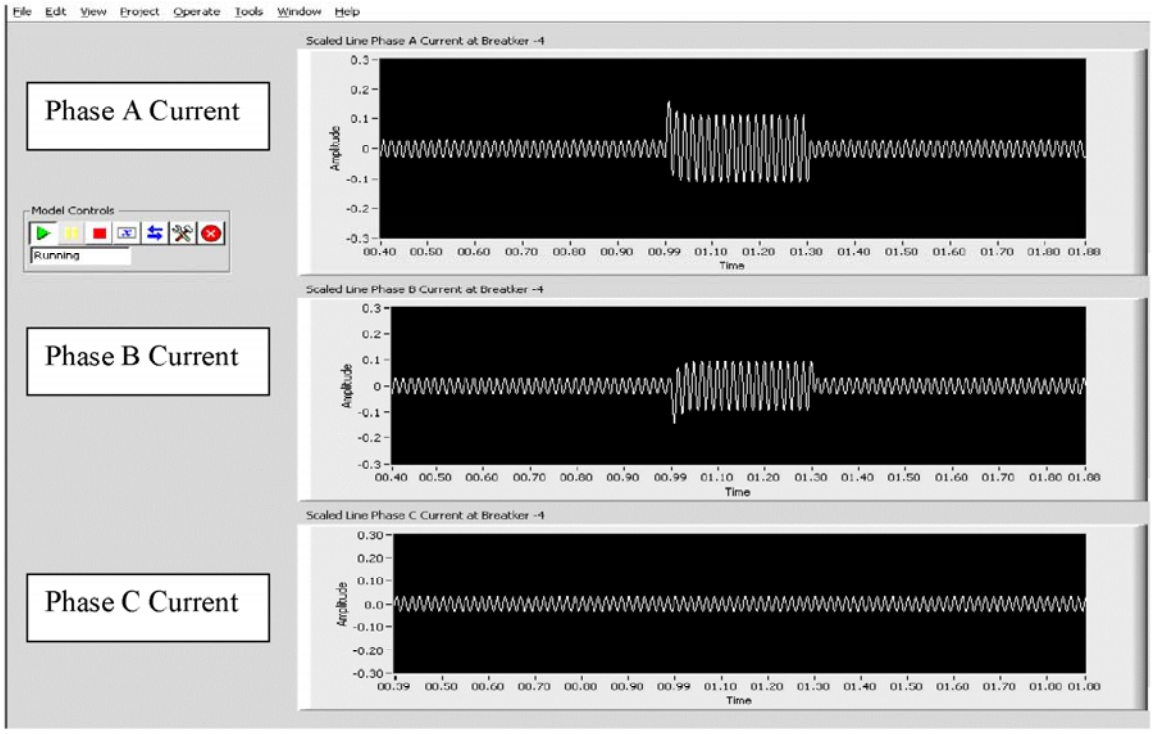


Figure 7.7 LabVIEW user interface showing L-L-G on phases A, B

The report taken from the SEL-351S for the simulated double line to ground fault on the NI-PXI shows that during fault, the phase A and phase B current increase above 960A where as phase C current is well below threshold [40].

The NI-PXI could simulate an eight-bus power system in real time and can function as a power system simulator. With the present configuration of the NI-PXI at Mississippi State University, systems as big as 10 to 12 buses can be simulated in real time. By doubling the RAM capacity, it can simulate even higher bus systems. The cost of NI-PXI is much less than the cost of RTDS. The RTDS simulator is dedicated to power systems simulations and can simulate bigger systems more efficiently and accurately than NI-PXI [40].

7.4 Closed loop testing between NI-PXI and dSPACE

7.4.1 Introduction

In this section, closed loop testing is done between the NI-PXI and dSPACE with the power system running in real-time on the NI-PXI and instantaneous overcurrent relay model running on dSPACE board. Figure 7.8 shows the setup of the closed loop test between the NI-PXI and dSPACE at MSU PERL.

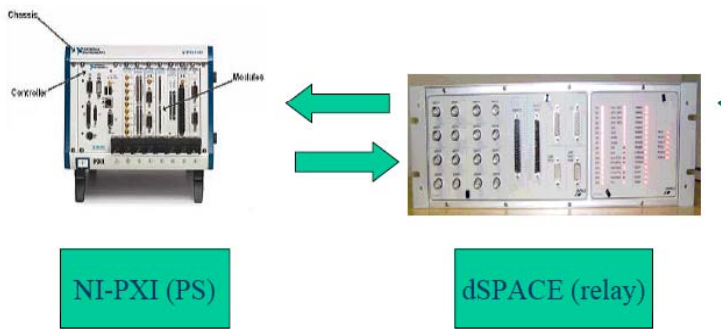


Figure 7.8 Setup of the closed loop test between NI-PXI and dSPACE

7.4.2 dSPACE relay model

An instantaneous overcurrent relay model is developed and implemented on the dSPACE-1104 controller. The overcurrent relay modeling is done in Matlab/Simulink. The model is later deployed into the dSPACE controller board to run it in real-time. This relay model is flexible and the user can define its threshold current (pick up current) for the relay model as well as delay between trip and reclose signals. The trip and reclose signals given by the relay are Transistor–Transistor Logic (TTL) in nature with high being in the range of 5V-2.2V and low being 0V-0.8V [42]. For this closed loop testing between NI-PXI and dSPACE, the threshold current is set to 5A, and the delay between trip and reclose signal is 0.25 secs [22] [43].

7.4.3 Signal Connections between NI-PXI and dSPACE

The Matlab/Simulink power system models described in chapter V for SIL testing are run in real-time on NI-PXI. The NI-PXI 1042Q chassis present at MSU PERL has the NI-PXI 6733 DAQ card in slot-2 and the NI-PXI 6251 DAQ card in slot-5. The NI-PXI 6733 is a high-speed analog output card. The three phase currents coming from the CT

secondary are fed into the dSPACE relay using the NI-PXI 6733 card. A standard sampling period of 1000 samples/sec is used. Figure 7.9 shows the configured channels of the NI-PXI 6733 for three-phase current coming out of CT sec. The trip and reclose signals generated by the dSPACE relay model are connected to the NI-PXI 6251, multi-functional DAQ card. Figure 7.10 shows the configured channels of the NI-PXI 6251. Differential mode of data acquisition is used for collecting the trip and reclose signals.

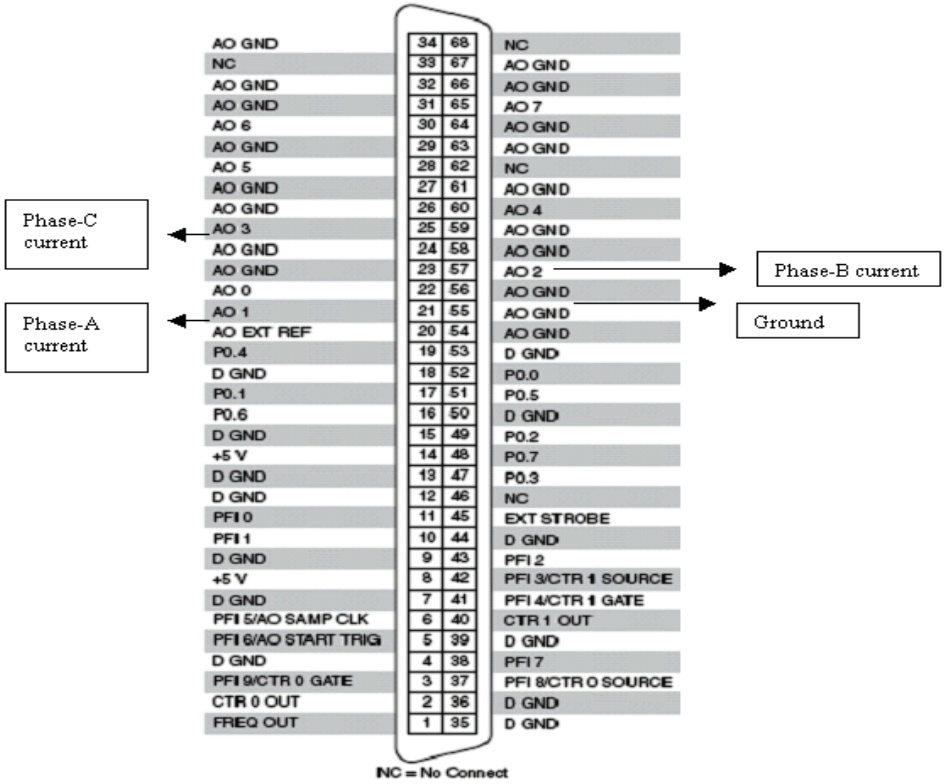


Figure 7.9 Pin out for NI-PXI 6733 [44].

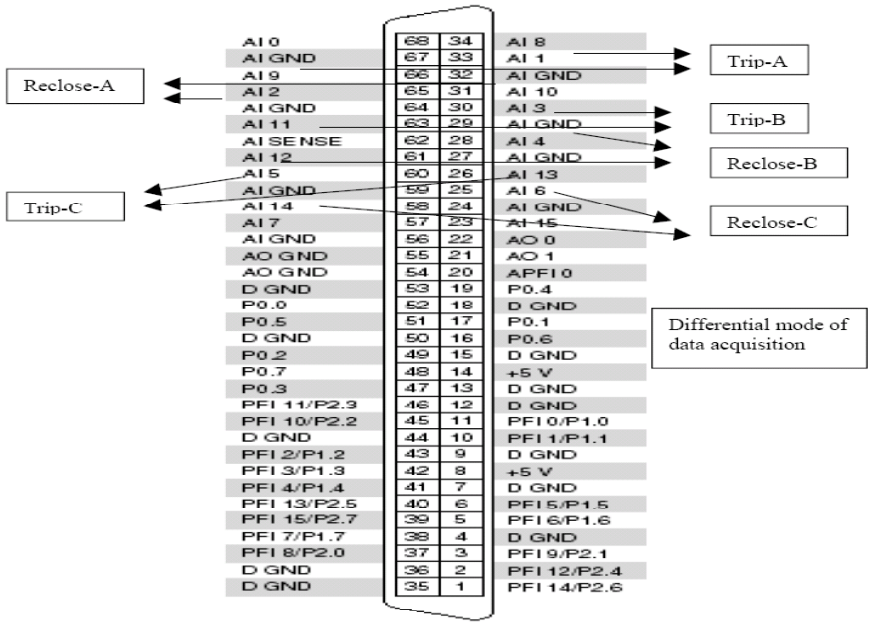


Figure 7.10 Configured channels of NI-PXI 6251 for trip and reclose signals [37]

7.4.4 Closed loop test results with two-bus power system

As a base case, a two-bus power system is used to conduct the closed loop test. The two-bus power system used here is same as the one used for SIL testing in section 5.3.1, chapter V. The current and voltage signals are scaled down to make sure they are within DAQ card ranges.

7.4.4.1 L-G fault

A single phase to ground fault is placed on the two-bus power system at 4.0 secs. Figure 7.11 shows the screenshot of closed loop test for an L-G fault on phase-A on a two-bus power system.

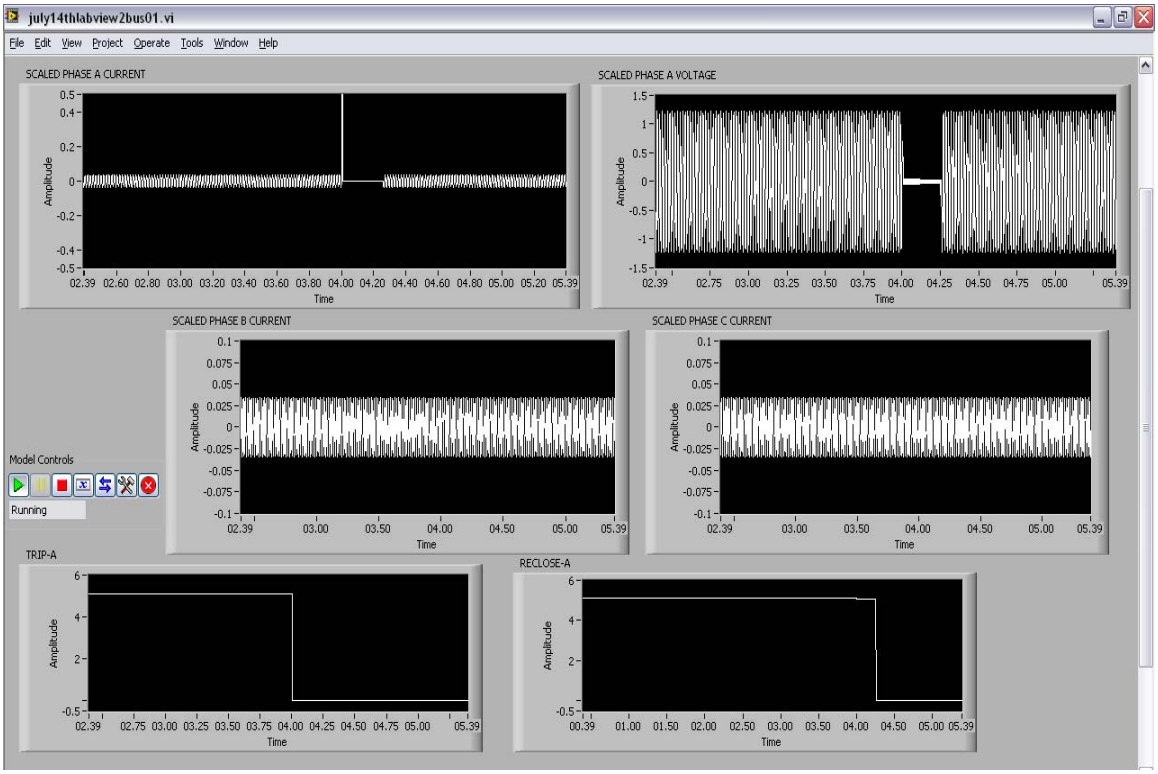


Figure 7.11 Result of closed loop test for an L-G fault on phase-A on a two-bus

The figure shows scaled currents for all the phases, scaled phase-A voltage, trip signal for phase-A, and reclose signal for phase-A. It is evident from the figure that the fault is cleared within half-a cycle of occurrence of the fault. The trip signal is generated instantaneous. The reclose signal is generated at 4.25 secs and after that system is reclosed.

7.4.4.2 L-L-G fault

A double line to ground fault is placed on phases A and B of the two-bus power system at 4.0 secs. Figure 7.12 shows the screenshot of closed loop test for an L-L-G fault on a two-bus power system.

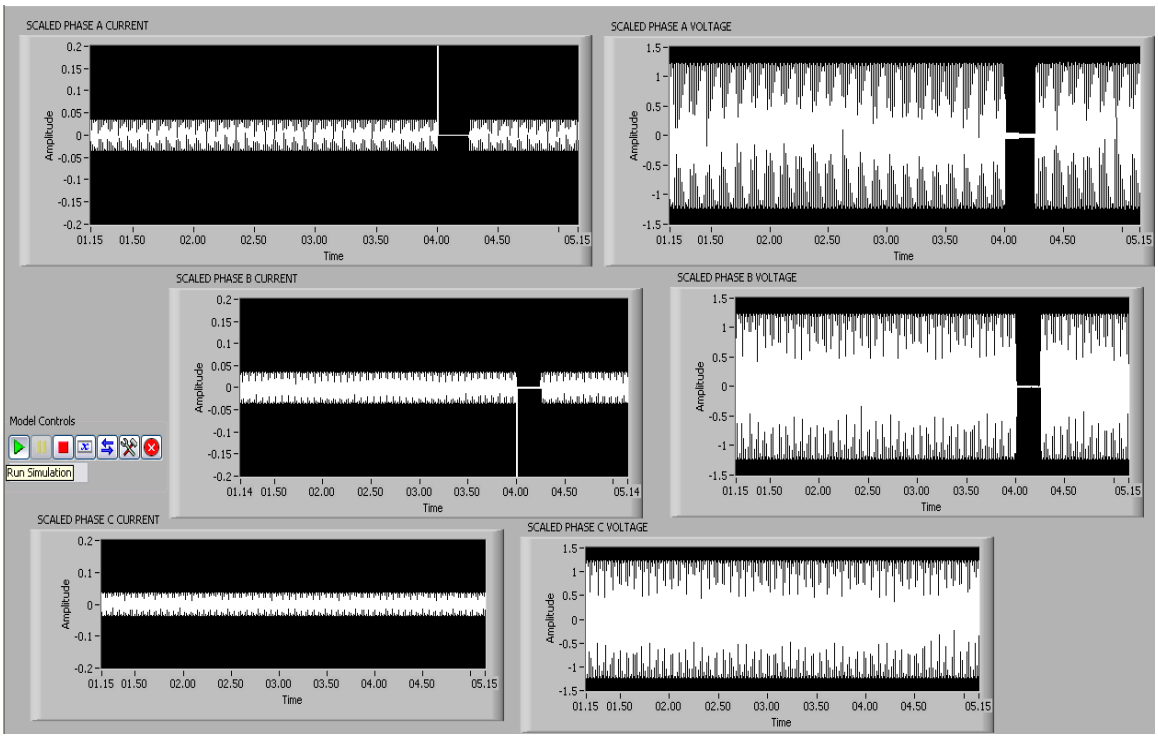


Figure 7.12 Result of closed loop test for L-L-G fault on two-bus power system.

Graphs of scaled currents for all the phases, and scaled voltages of all the phases are presented in the screenshot. From the figure, it is evident that the fault is cleared within half-a cycle and the system is reclosed at 4.25 secs.

7.4.5 Closed loop test results with Shipboard power system

After testing with a two-bus power system, analysis has been done with a SPS. The SPS used here is same as the one used in section 5.3.3, chapter V. An L-G fault is placed on phase-A of the SPS near bus-3 (figure 3.6, chapter III). The fault is injected into the system at 3.0 secs.

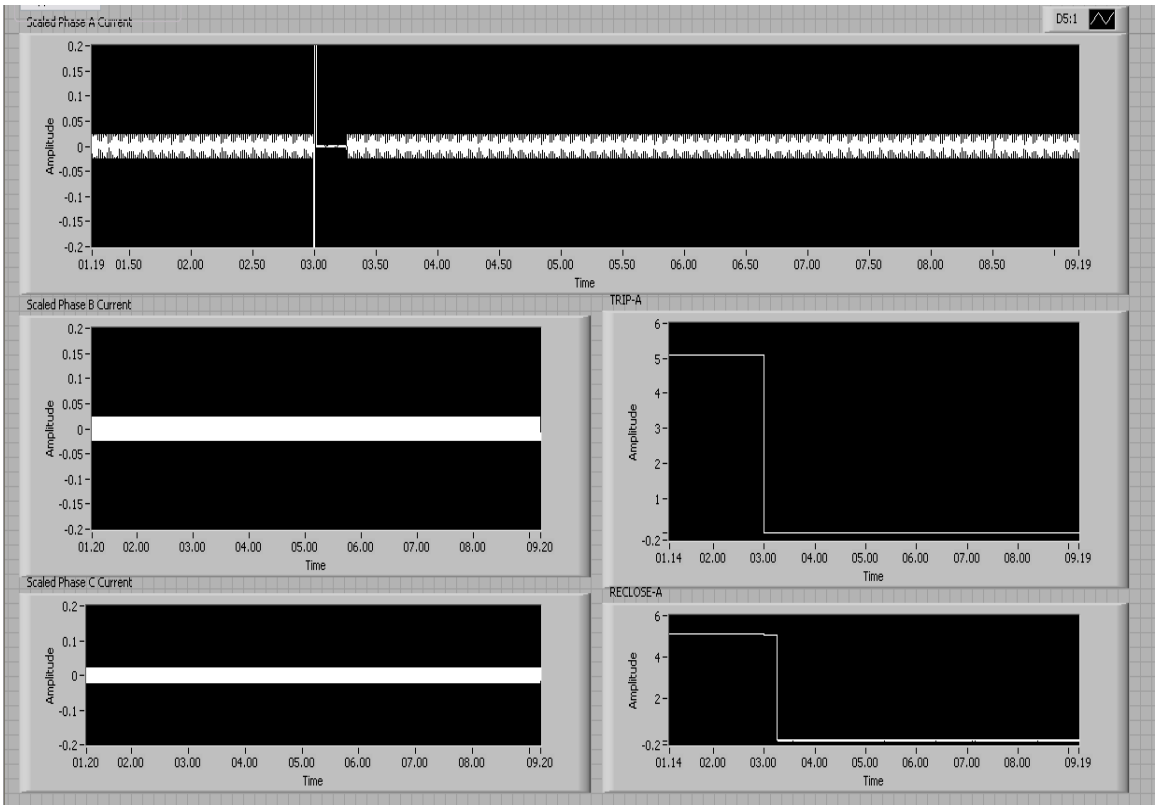


Figure 7.13 Results of closed loop testing on SPS for L-G fault.

Figure 7.13 shows the screenshot of closed loop testing on SPS. The dSPACE relay detects the fault and clears it after 1 cycle of fault period. The system is reclosed at 3.25 secs with the intervention of reclose signal.

7.5 Hardware-in-the-Loop testing between NI-PXI and SEL-351S Relay

7.5.1 Introduction

To even make the developed real-time HIL platform stronger, a HIL test is conducted between the NI-PXI (acting as power system simulator) and the SEL-351S

relay. Figure 7.14 shows the HIL test setup at MSU PERL. The HIL test is conducted for two-bus power system model running on NI-PXI controller for different fault scenarios.

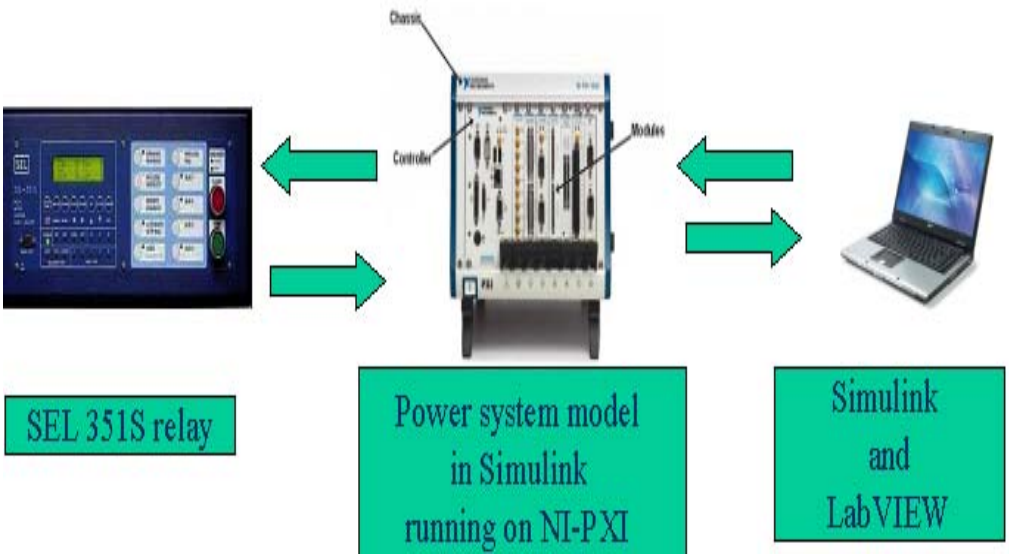


Figure 7.14 HIL test setup at MSU PERL.

7.5.2 SEL-351S Relay

SEL-351S relay is a protection and breaker control relay. This relay has numerous operator controls, under/over frequency protection, trip and reclose push buttons along with LEDs, supports communications etc [41]. In this test, the directionality component is switched off for reducing complexity. The threshold current is set at 960A and the relay trips all the three phases even for a single line to ground fault or a double line to ground fault.

7.5.3 Signal connections between NI-PXI controller and SEL relay

The three analog voltages and three analog currents along with ground signal coming from the NI-PXI is provided to the SEL351S relay through the NI-PXI 6733 high-speed analog output. The signals drawn from the NI-PXI 6733 device in this HIL test are similar to the way mentioned in section 7.4.2, Figure 7.9. Apart from the currents, voltage signals are also fed into the SEL-351S relay. Phase-A voltage is provided from channel AO-4, phase-B voltage is provided from channel-AO-5, and phase-C voltage is provided from channel AO-6. The trip and reclose signals coming from the SEL-351S relay are fed back into NI-PXI controller through NI-PXI 6251 DAQ card in the same way described in section 7.4.2, figure 7.10.

7.5.4 HIL testing for two-bus power system

The two-bus power system model used here is same as the one used for the SIL testing in section 5.3.1, chapter V.

7.5.4.1 L-G Fault

An L-G fault is injected into the two-bus power system at 4.0 secs. The fault duration is from 4.0 secs to 4.50 secs. Figure 7.15 shows the HIL test result for L-G fault.

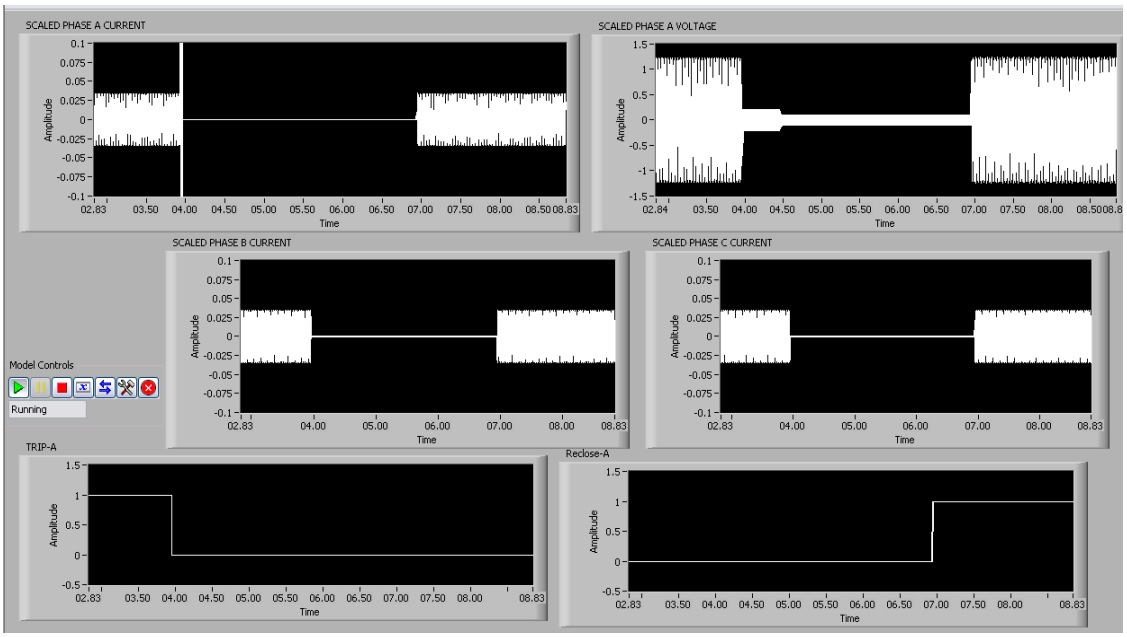


Figure 7.15 HIL test results for two-bus system for L-G fault

The LabVIEW screenshot shows Phase-A current and voltage, phase-B, phase-C currents, trip and reclose signals. After occurrence of the fault, the SEL-351S relay detects the fault with-in 2 cycles and trips the system. The system is reclosed at 7.0 secs. It is observed that for a single line to ground fault, all the three phase are tripped by the SEL relay.

7.5.4.2 L-L-G Fault

A similar HIL testing is done between the NI-PXI and SEL-351S relay on the two-bus system for a L-L-G fault. Figure 7.16 shows the HIL test result. The LabVIEW screenshot shows the three single-phase currents and three single-phase voltages. The fault occurs at 4.0 secs and the system is tripped after 2 cycles. The system reclosed at 7.0 secs.

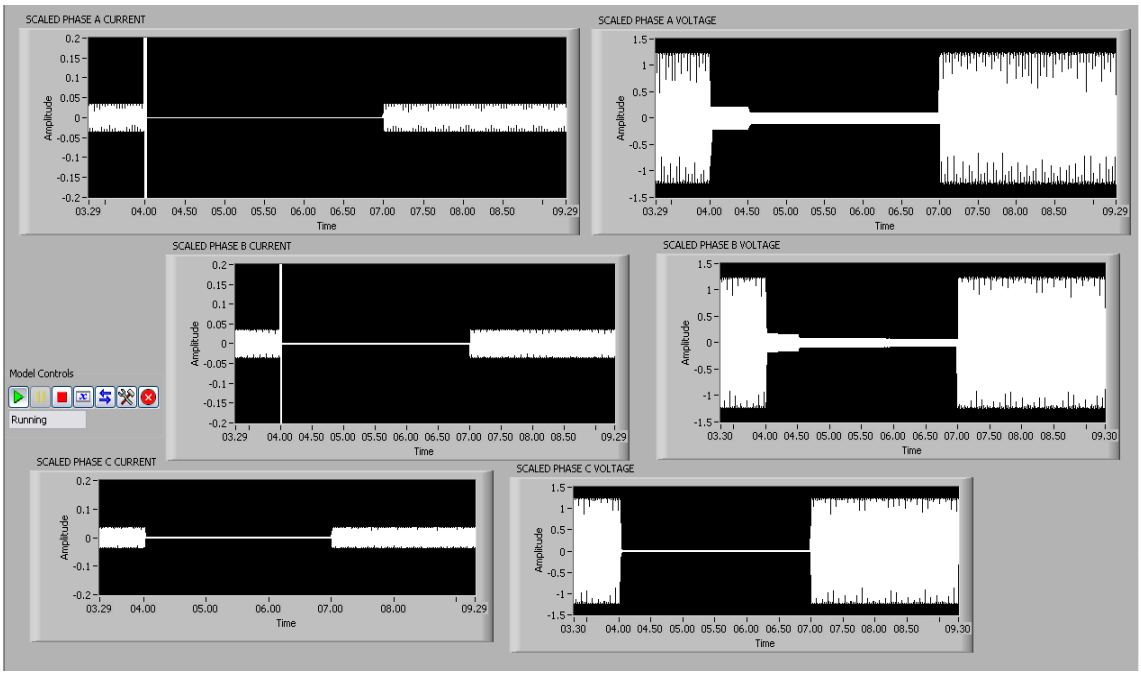


Figure 7.16 HIL test results for two-bus system for L-L-G fault

7.6 Summary

In this chapter, the procedure followed to develop a HIL platform using NI-PXI is presented. Using that HIL platform, efforts have been placed to establish NI-PXI as a power system simulator. The results of closed loop tests done on the developed HIL platform with different power systems and dSPACE relay model are presented. The results of HIL test conducted between NI-PXI and SEL-351S relay are also presented.

CHAPTER VIII

CONCLUSIONS AND FUTURE WORK

8.1 Conclusions

Protective relaying is an open area where there is always a room for development. Especially, the advancements in real-time protective modeling are always possible and needs more research. This thesis work addressed the development of flexible overcurrent relay model using LabVIEW that can be used in two operational modes. The additional features present in the relay model prove to be extremely useful to depict the performance of a commercial relay. The NICIL and SELRIL test suite validates the relay model and concludes that the relay model is a first order approximation of the commercial relay and provides an opportunity for testing and analysis in real-time.

This thesis work also contributes towards developing a NI-PXI platform for power system simulation. The scope of application of the NI-PXI is huge including electrical, mechanical, chemical, biological and other engineering fields. NI-PXI is an economical platform when compared to RTDS for power system simulations. Two-bus, eight-bus and SPS models are developed in Matlab/Simulink and run in real-time on NI-PXI controller. Modeling in Simulink does not offer as many details about the power system components as in RSCAD or VTB. A PSS based on Matlab/Simulink and PXI platform has better customer support for any technical issues than RTDS or VTB.

Since RTDS was being dedicated to real-time power system simulation, it offers much better performance and accuracy compared to the NI-PXI PSS. Performance of the NI-PXI system for power system simulations has been tested by conducting open loop tests with SEL-351S relay and comparing the results with the open loop test results conducted on RTDS. HIL tests are also conducted with a SEL-351S relay and dSPACE overcurrent relay model. The test results are helpful in providing validation of the device design. The platform set-up for the NI-PXI is tedious as compared to VTB and RTDS. Using the NI-PXI as a power system simulator makes a compromise between cost and degree of real-time simulation accuracy.

8.2 Future Work

This thesis work has provided a first order approximation of the overcurrent relay as a LabVIEW model. There are several opportunities to extend the functionality and capabilities of the relay model for advanced capabilities. An example of this is adding the feature of directional overcurrent capabilities. The relay model can also be modified to include additional blocks that allow conversion to other types of relays such as differential or distance relays. Data logging capabilities could be incorporated to help with post-fault analysis. The other next step related to this work is to duplicate the model and incorporate multiple relay models within the test system. This will involve more advanced relay coordination. This will also allow for optimization strategies where both the power system and the protection system are considered.

The second part of thesis work concentrates on developing a Power System Simulator using National Instruments (NIPSS) and development of Hardware-in-the-Loop (HIL) platform. In this research, HIL platform testing is confined to overcurrent relays. This platform can be extended to testing of differential relay and distance relay. LabVIEW Math script allows modeling and simulation using Matlab m-files and LabVIEW together. This opens up broader scope of research and an option to deploy the code on NI-PXI system for running in real-time. If Matlab m-files are successfully run in real-time on NI-PXI then the reconfiguration scheme [45] developed by MSU alumni Oluwaseun A. Amoda can be implemented in real-time and his suggested future work can be completed with ease. Development of NIPSS and HIL platform is done using LabVIEW and Matlab/Simulink. The diverse library of Simulink makes this platform available to areas other than power systems and power electronics.

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